

# Compal Confidential

## Schematics Document

Intel

ARRANDALE with IBEX PEAK-M

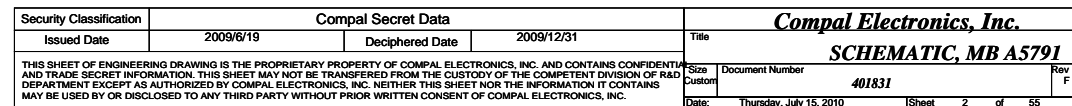
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LA-5792P

2010-06-21

REV:1.0

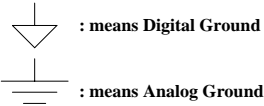
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Voltage Rails ( O MEANS ON X MEANS OFF )

<div>power plane</div> <div>State</div>	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.05VM_LAN	+3VM +1.05VM	+1.5V +1.05V +3V	+5VS +3VS +1.5VS +VCC_GFXCORE +VCCP +CPU_CORE +1.05VS +1.8VS +0.75VS +1.2VS
S0	O	O	O	O	O	O	O
S3 / DC	O	O	O	O	X	O	X
S3 / AC	O	O	O	O	O	O	X
S3 / S4 / S5 WoLAN	O	O	O	O	X	X	X
S5 S4/AC	O	O	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X	X

Symbol Note :



@ : means just reserve , no build  
CONN@ : means ME part.

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.2

LV: LV@+FEL@+LC@+HQE@+USB3@  
VA: VA@+LC@+SW@+LVDS@+USB2@  
VE: VA@+VE@+FEL@+LVDS@+USB2@  
LV WO/HQE USB3: LV@+FEL@+LC@+LVDS@+USB2@  
LV W/HQE WO/USB3: LV@+FEL@+LC@+HQE@+USB2@  
U3L(VA): VA@+LC@+SW@+LVDS@+USB2@  
U32(LV WO/HQE W/USB3): LV@+FEL@+LC@+LVDS@+USB3@

SMBUS Control Table

	SOURCE	BATT	XDp	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DAI	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	X	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	V	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	X

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

**JCPU1B**

COMP3  
COMP2  
COMP1  
COMP0

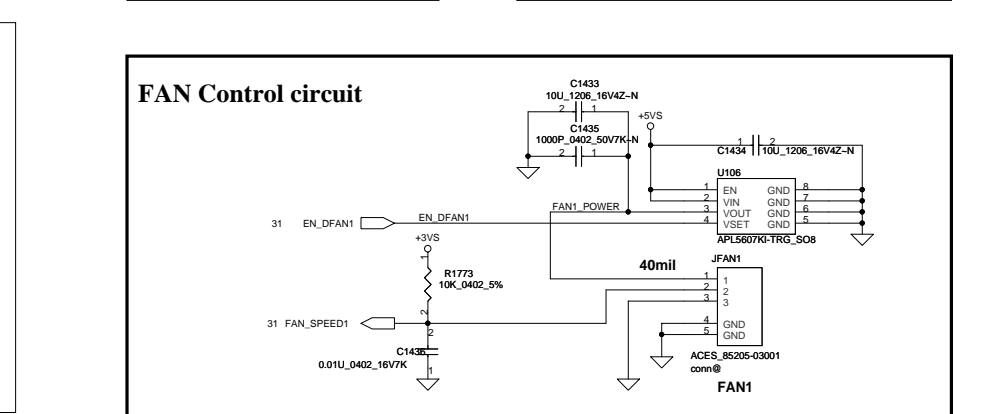
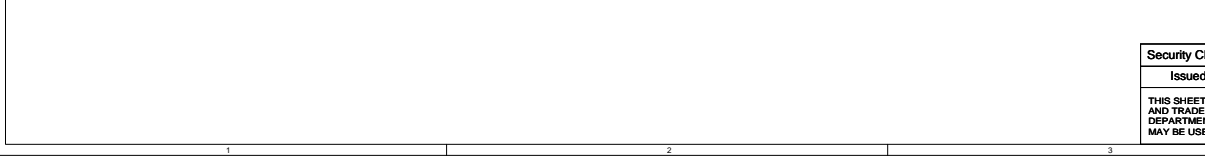
20 0402 1% 1 2 R2 COMP3 AT24  
20 0402 1% 1 2 R5 COMP2 AT24  
49.9 0402 1% 1 2 R7 COMP1 G16  
49.9 0402 1% 1 2 R9 COMP0 AT26

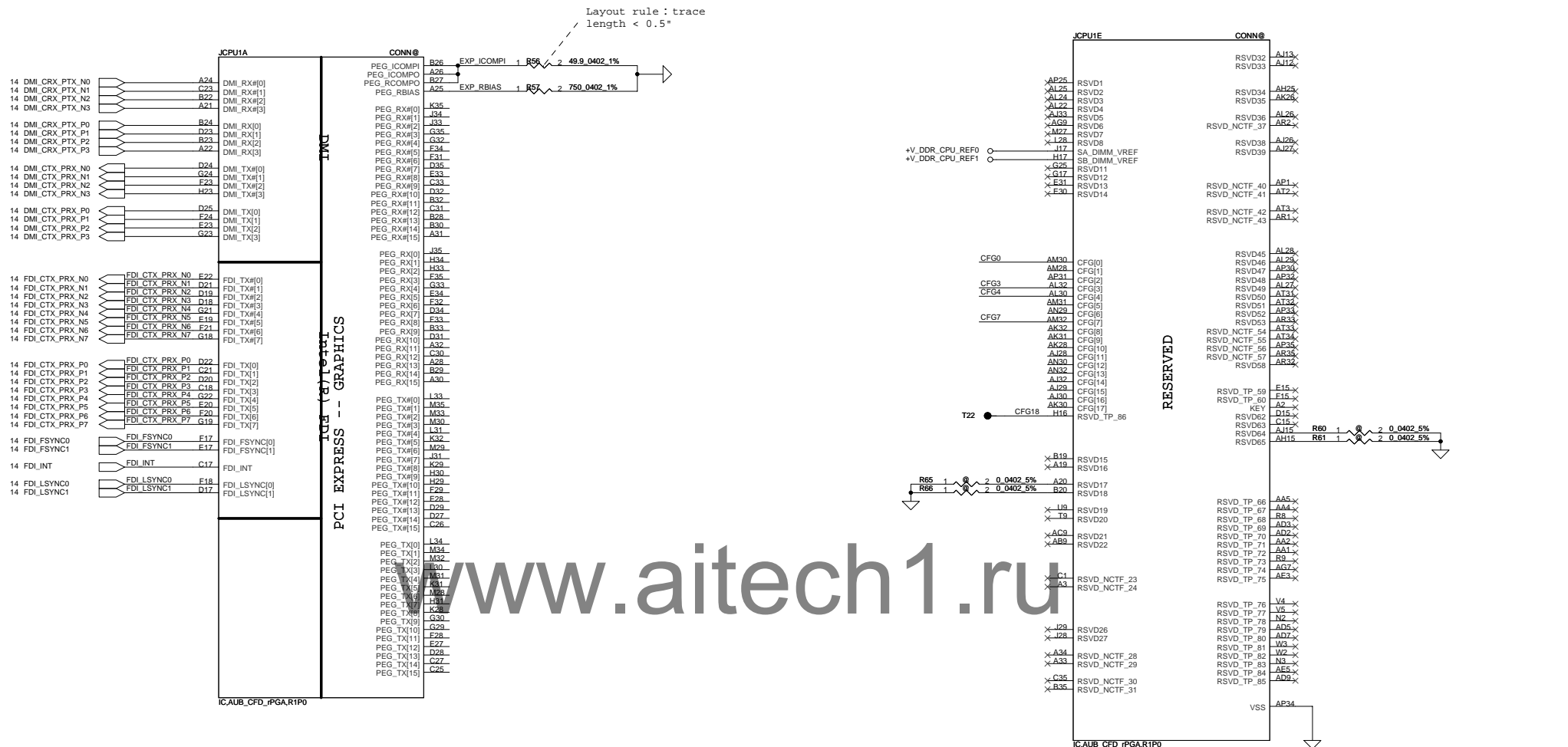
T2 TP\_SKTOCC# AH24 SKTOCC#  
H\_CATERR# AK14 CATERR#

15 H\_PECI R16 H\_PECI\_ISO AT15 PEGI  
14 H\_PROCHOT# H\_PROCHOT# AN26 PROCHOT#  
15 H\_THERMTRIP# R19 H\_THERMTRIP#\_R AK16 THERMTRIP#

to power, PU to VCCP at power side also  
44 H\_PROCHOT# H\_PROCHOT# AN26  
15 H\_THERMTRIP# R19 H\_THERMTRIP#\_R AK16

H\_CPURST# R20 H\_CPURST#\_R AP26 RESET\_OBS#  
14 H\_PM\_SYNC R21 H\_PM\_SYNC\_R AL15 PM\_SYNC  
H\_CUPWIRG R22 VCCPWRGOOD\_1 AN14 VCCPWRGOOD\_1  
15 H\_CUPWIRG R24 VCCPWRGOOD\_0 AN27 VCCPWRGOOD\_0  
14 PM\_DRAMP\_WIRG R25 VDDPWRGOOD\_R AK13 SM\_DRAMPWROK  
from power  
13 VTPWRGOOD VTPWRGOOD AM15  
H\_PWRGD\_XDP R30 H\_PWRGD\_XDP\_R AM26 TAPPWRGOOD  
15R 0402 1% 1 2 R33  
750 0402 1% 1 2  
BUF\_PLT\_RST# PLT\_RST#\_R AL14 RSTIN#  
IC\_AUB\_CFD\_IPGA\_R1P0





## CFG Straps for PROCESSOR

CFG0 R67 1 3.01K\_0402 1%

PCI-Express Configuration Select  
1: Single PEG  
CFG0 0: Bifurcation enabled  
Not applicable for Clarkfield Processor

CFG3 R69 1 3.01K\_0402 1%

CFG3-PCI Express Static Lane Reversal  
1: Normal Operation  
CFG3 0: Lane Numbers Reversed  
15 -> 0, 14 -> 1, ....

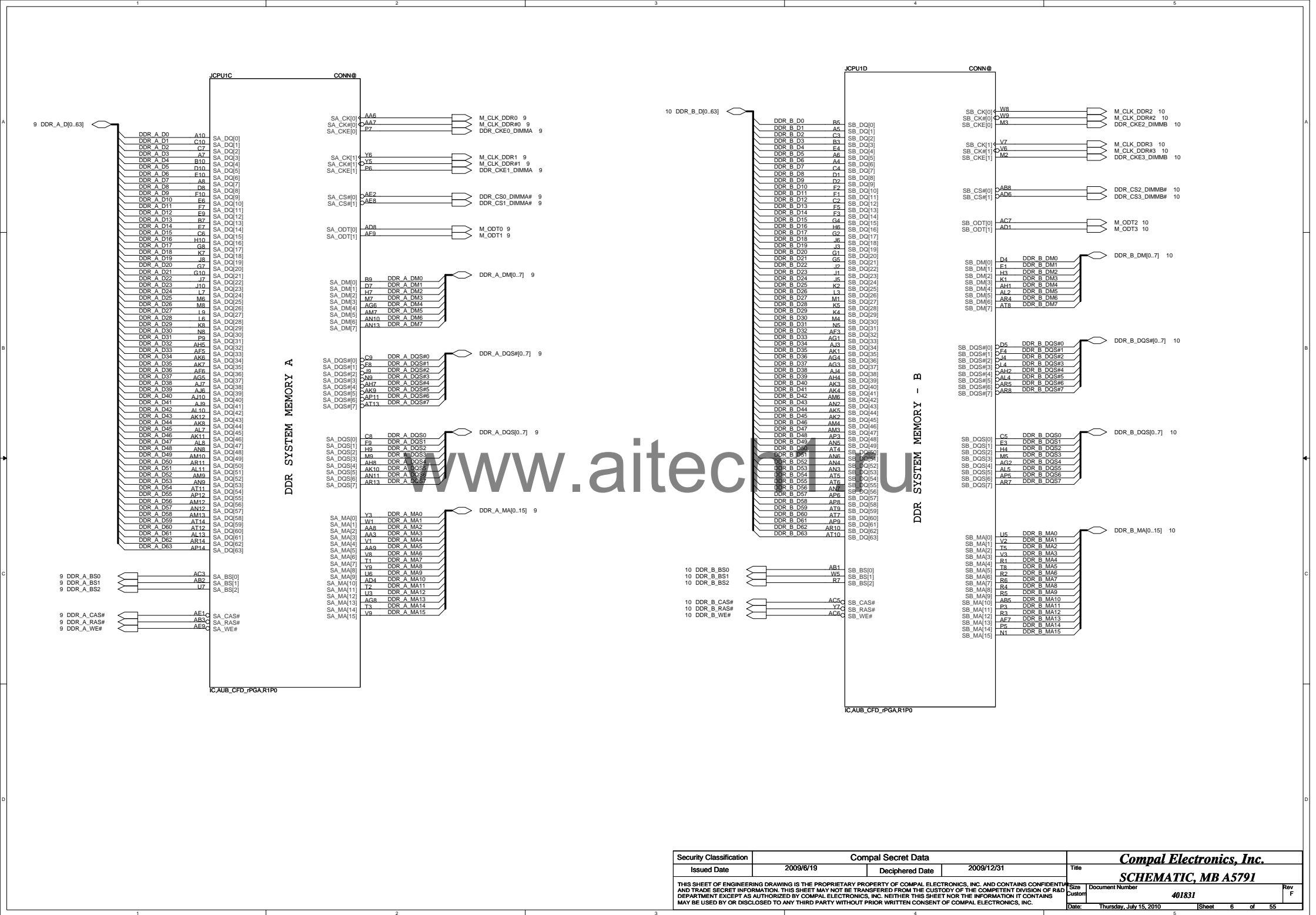
CFG4 R70 1 3.01K\_0402 1%

CFG4-Display Port Presence  
1: Disabled: No Physical Display Port  
attached to Embedded Display Port  
CFG4 0: Enabled: An external Display Port  
device is connected to the Embedded  
Display Port

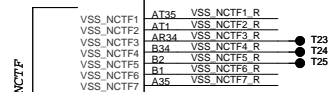
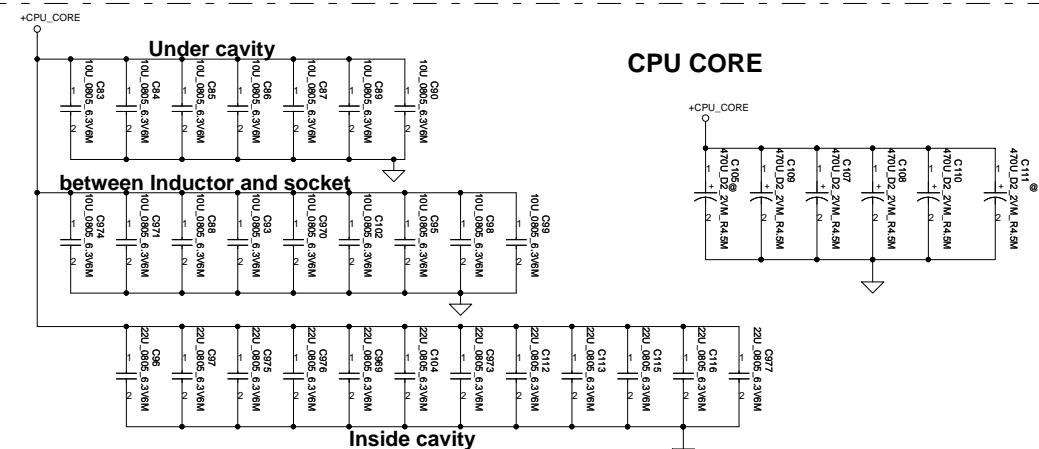
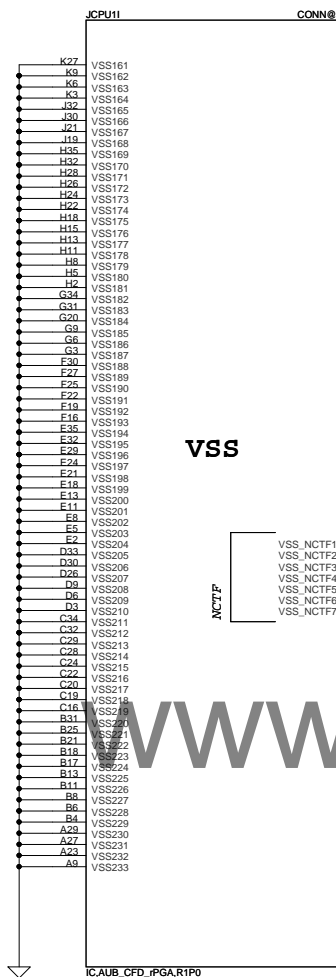
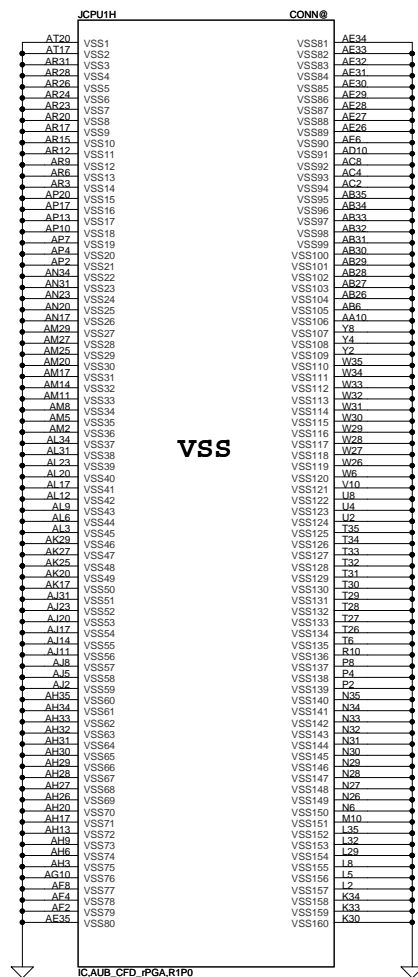
CFG7 R68 1 3.01K\_0402 1%

Only temporary for early CFD samples (rPGA/BGA)

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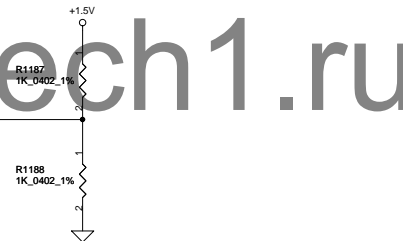
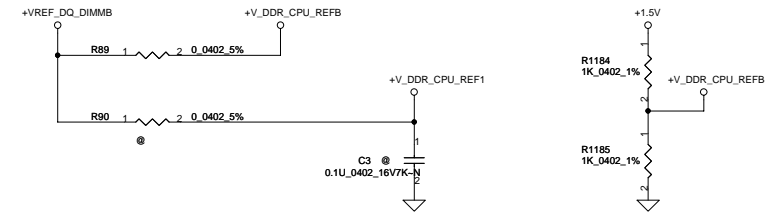
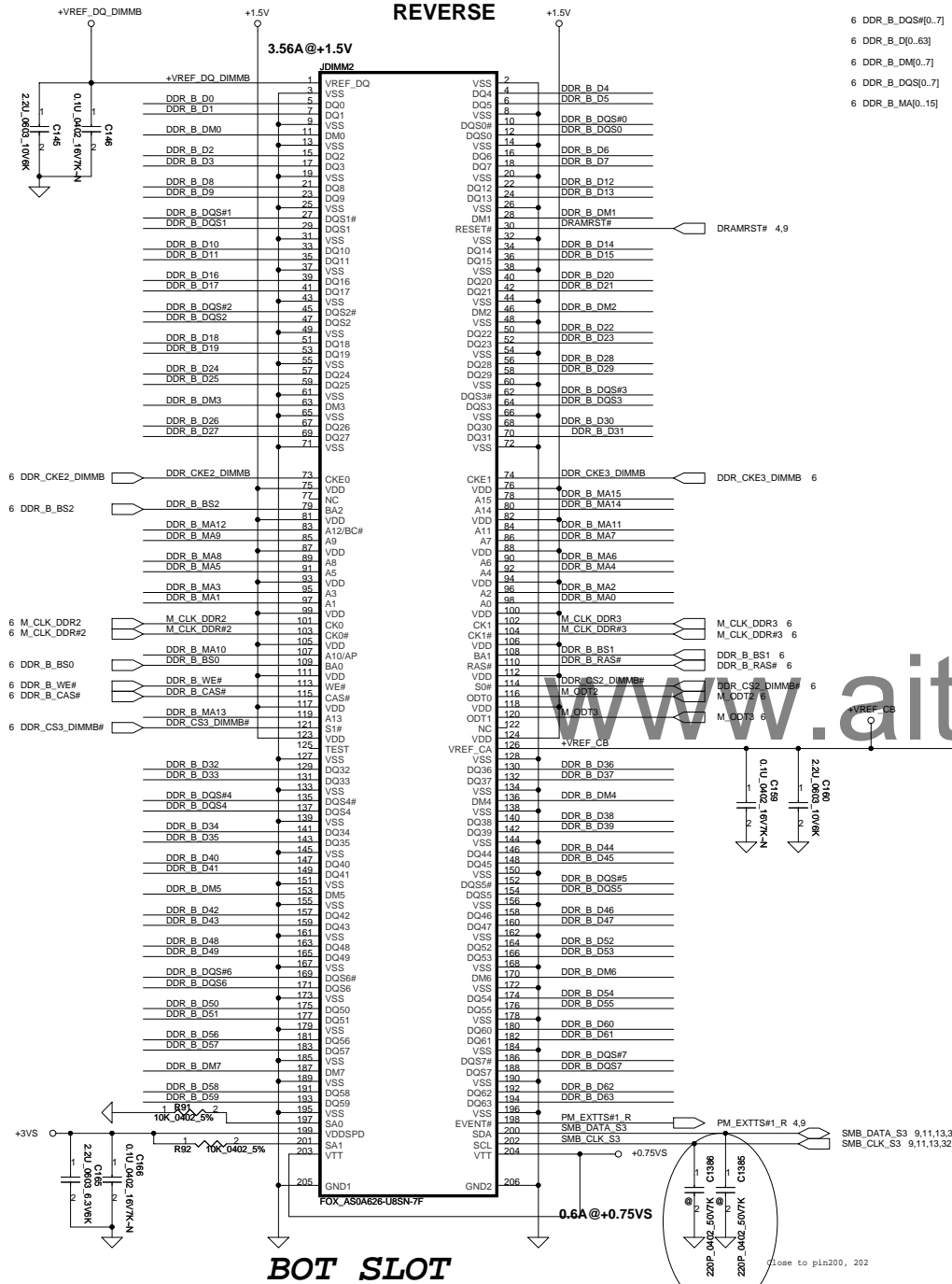
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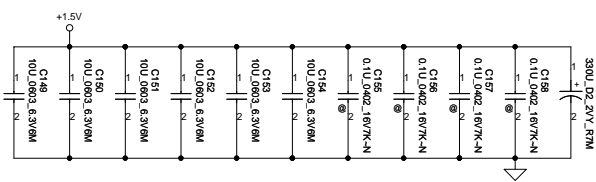




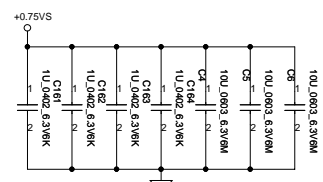
**DDR3 SO-DIMM B**  
**REVERSE** +1.5V



**Layout Note:**  
Place near JDIMMB

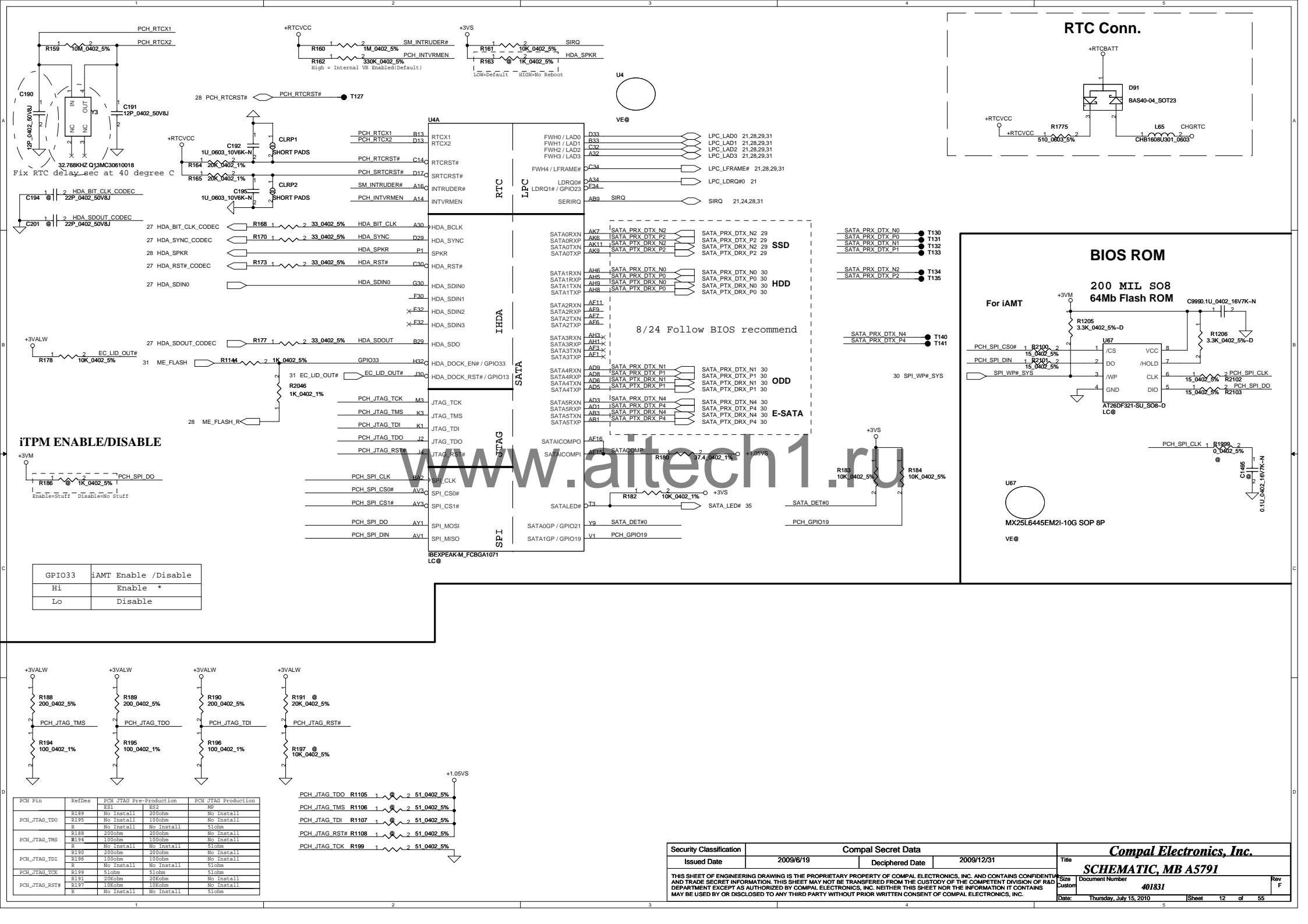


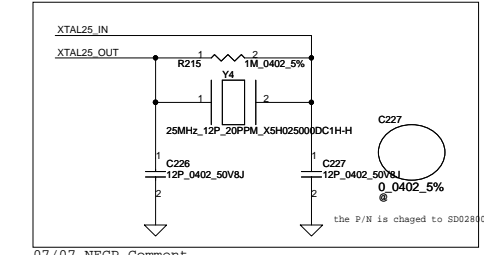
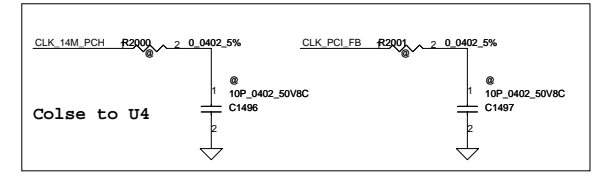
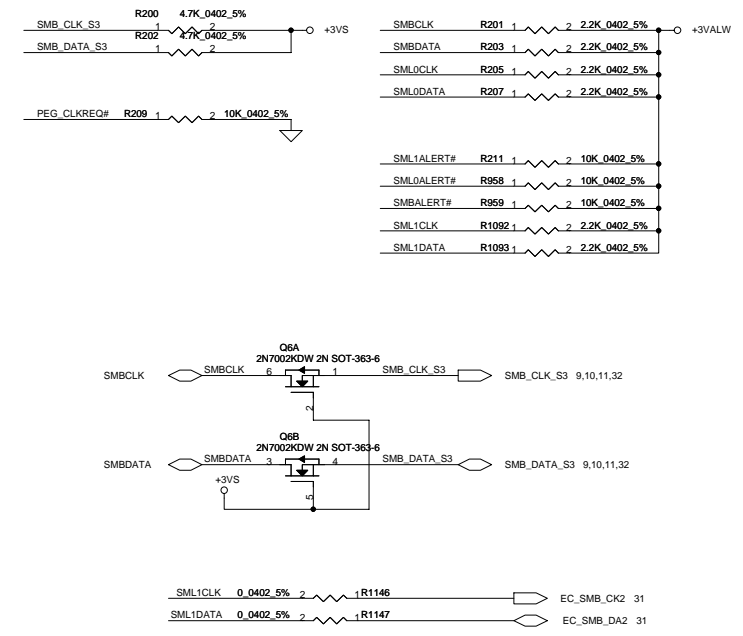
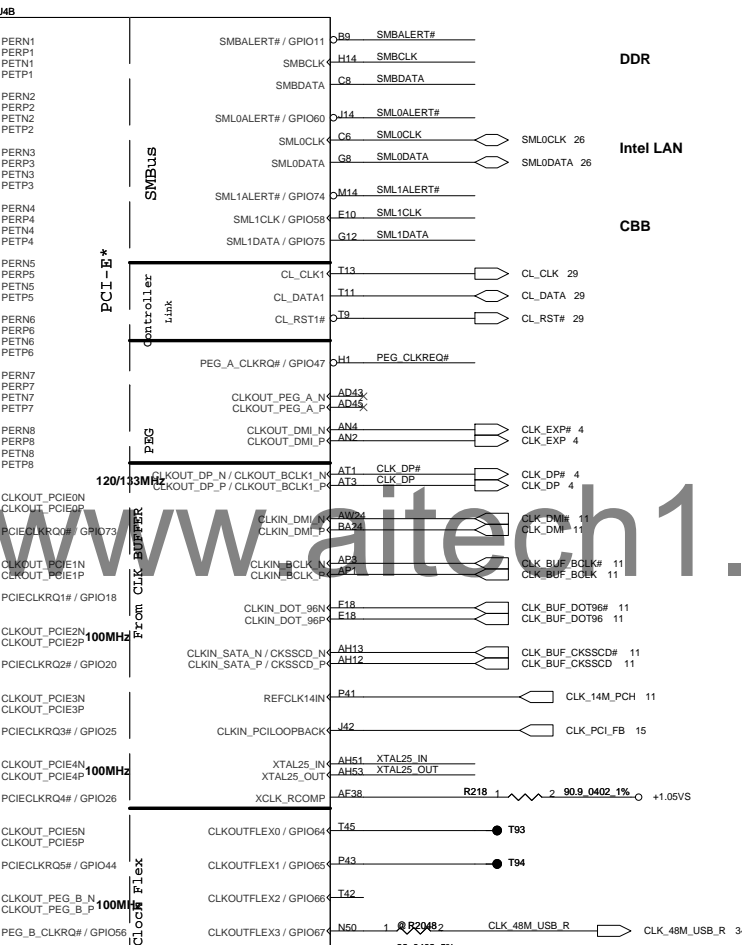
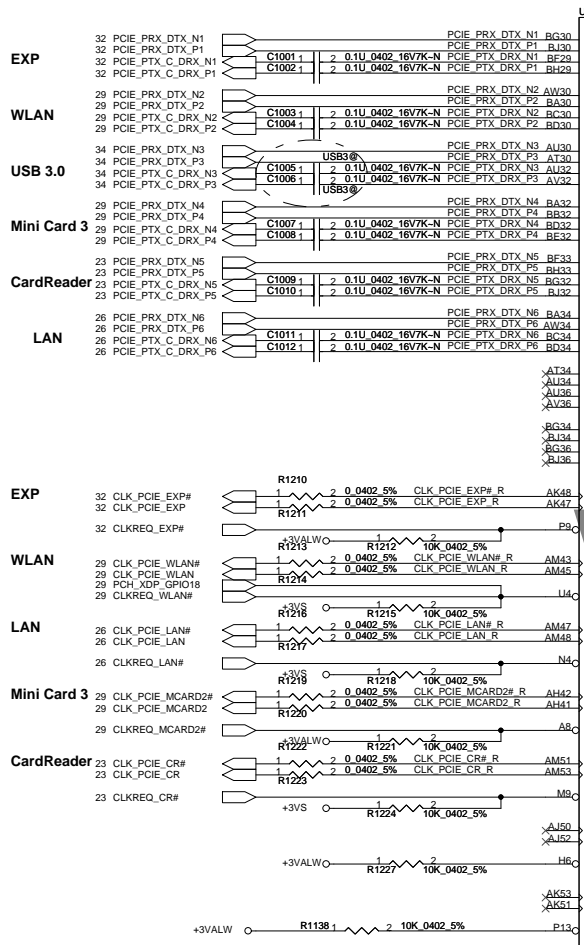
**Layout Note:**  
Place near JDIMMB.203 & JDIMMB.204



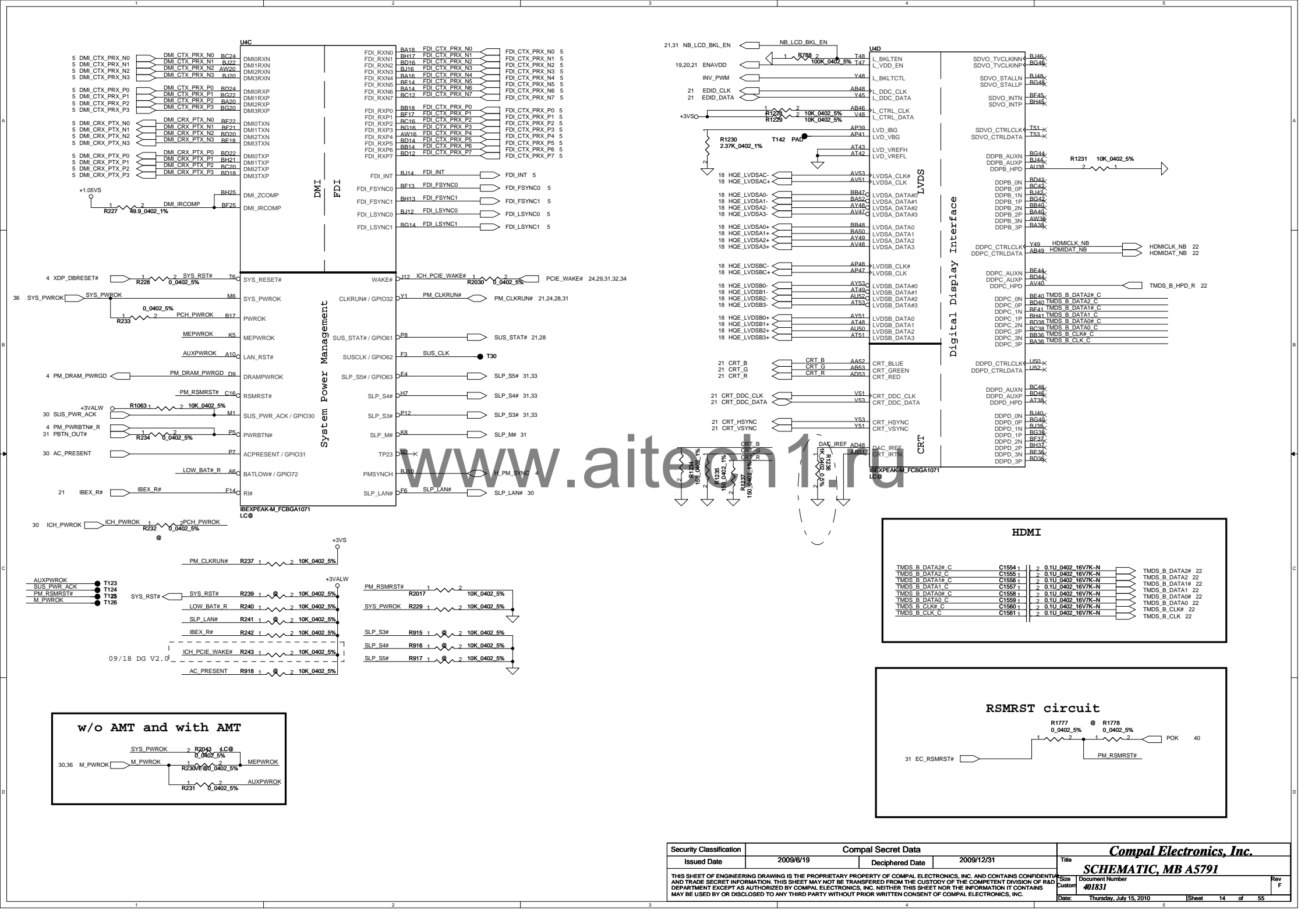
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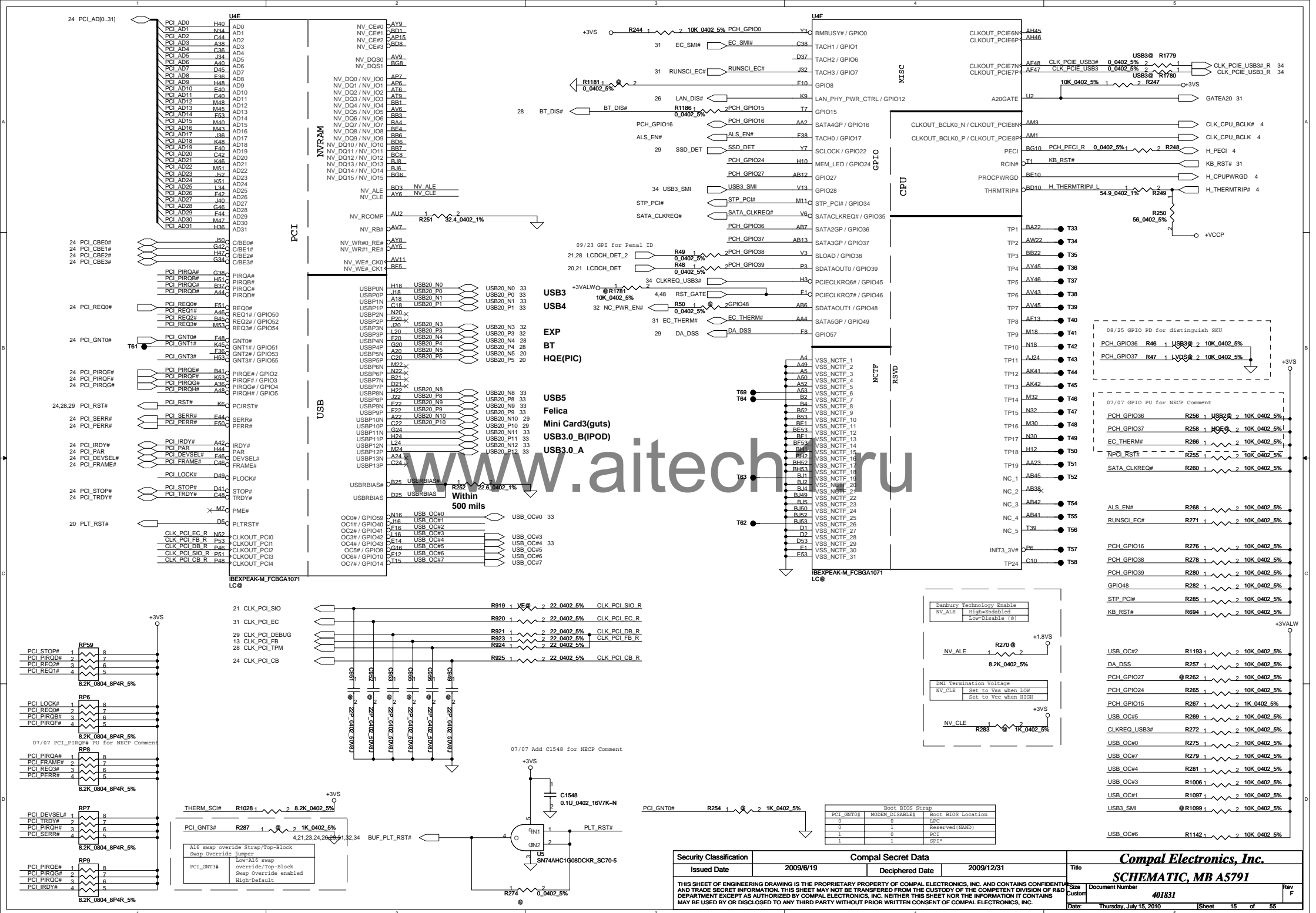




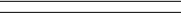


For USB3.0 48MHz CLK out



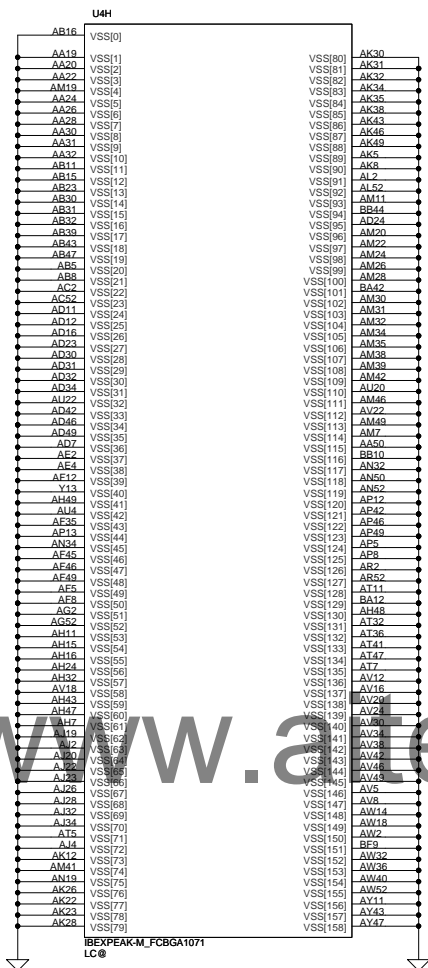
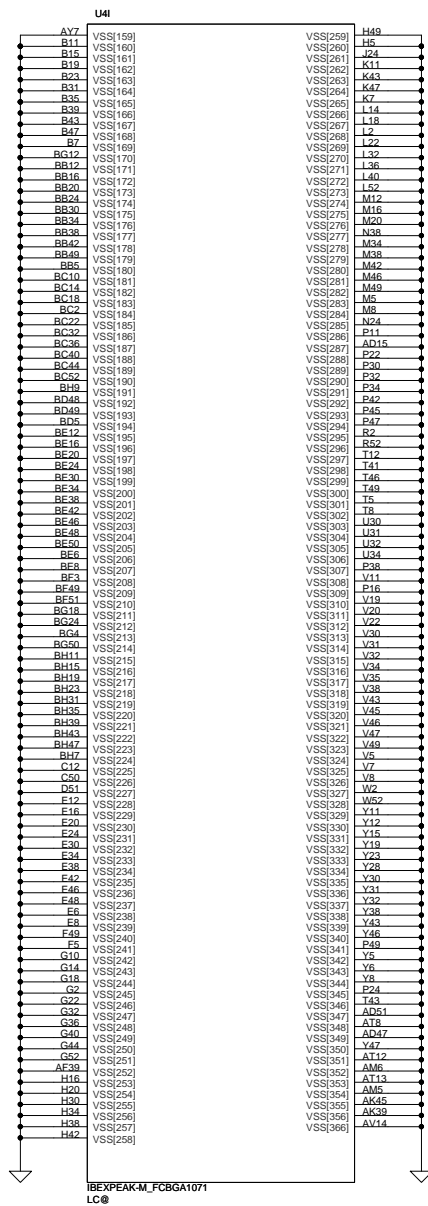


09/18 DG V2.0



1

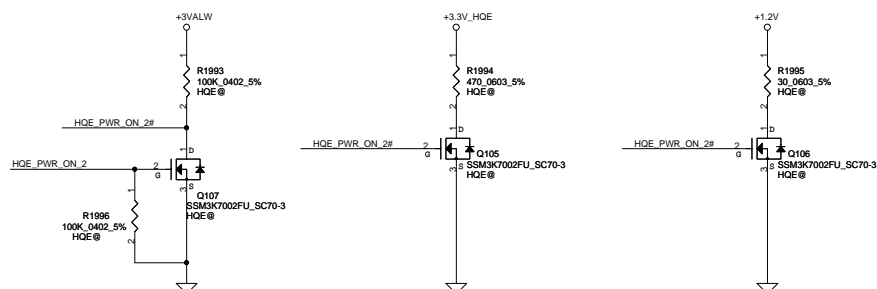
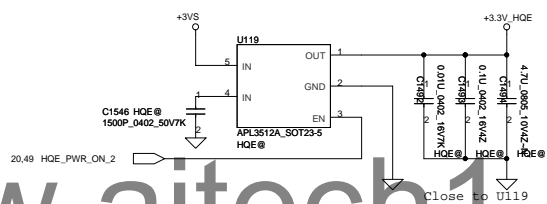
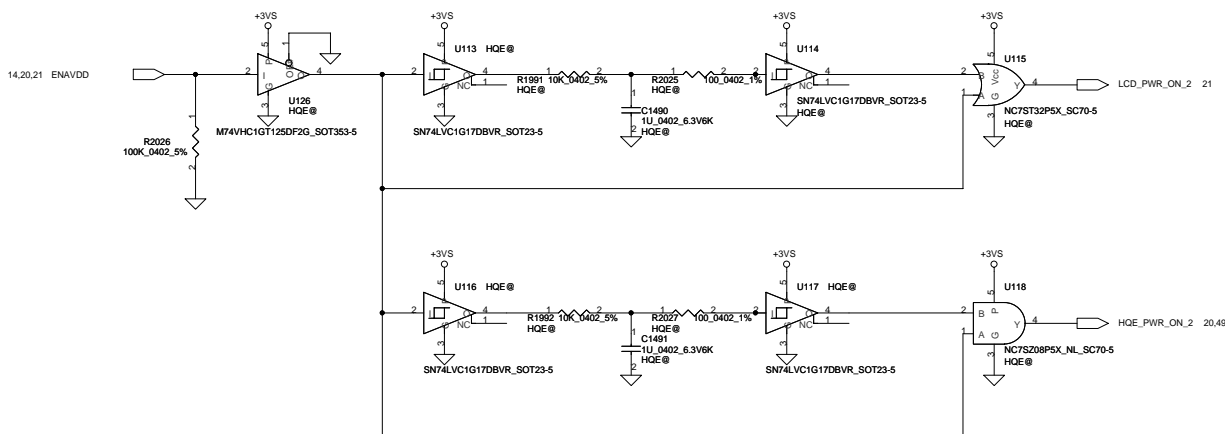


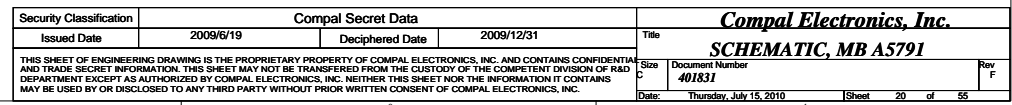


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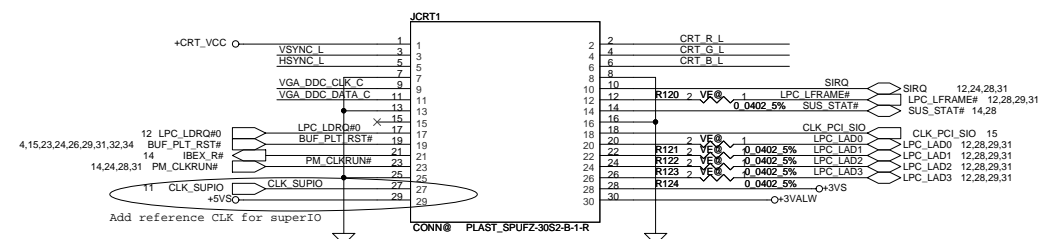
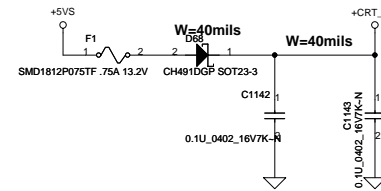
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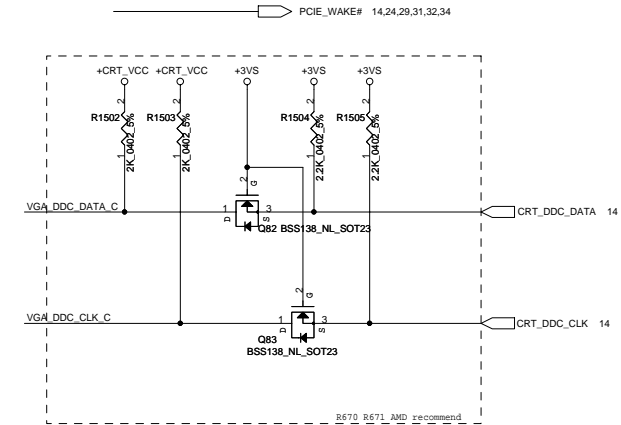
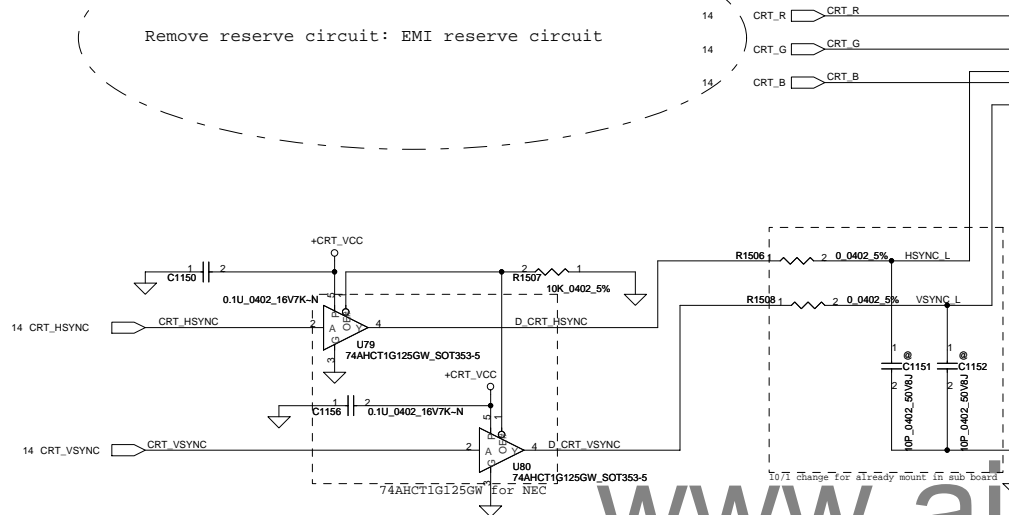
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# CRT

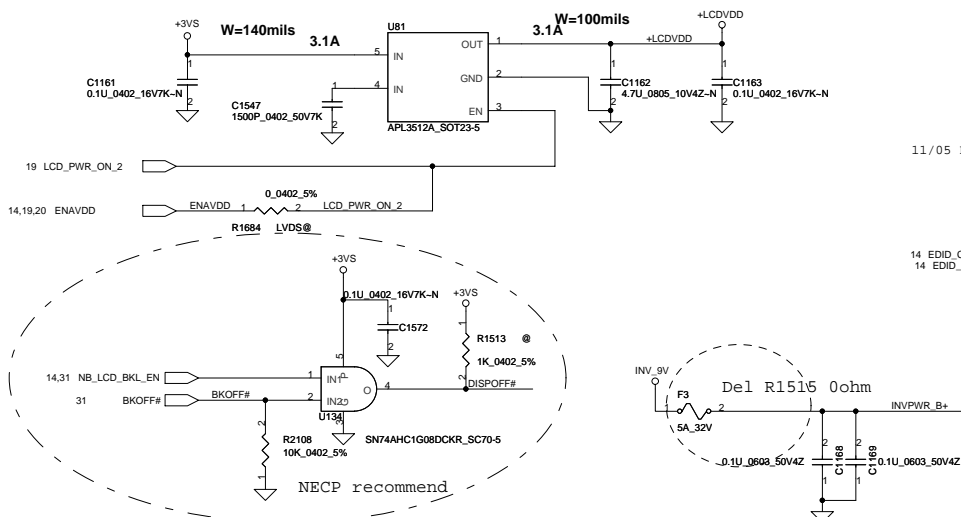


Remove reserve circuit: EMI reserve circuit

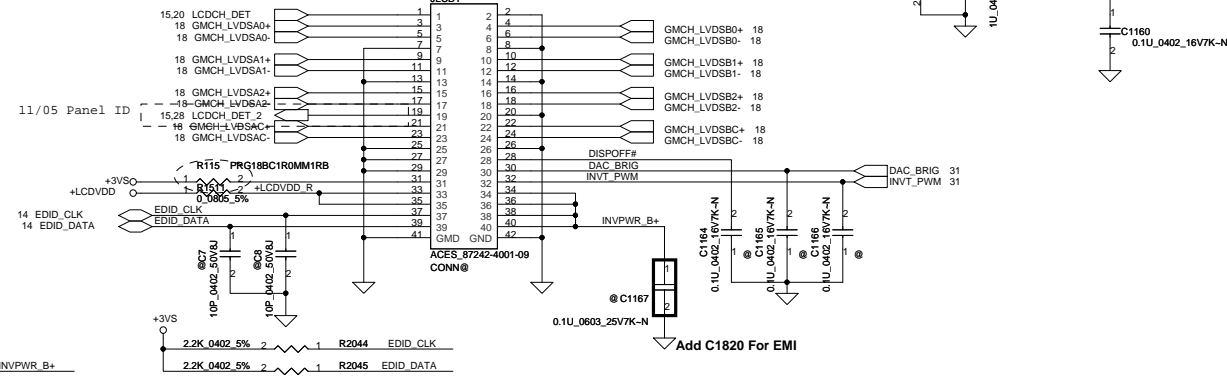


# LCD

## LCD POWER CIRCUIT



## LCDCH\_DET L: Dual-Link H: Single-Link



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EQUALIZATION SETTING:  
 [PC1,PC0]=00,8dB  
 [PC1,PC0]=01,4dB (Recommended)  
 [PC1,PC0]=10,12dB  
 [PC1,PC0]=11,0dB

Follow Intel  
 Feedback putting  
 2.2K ohm

0824 EMI requirement

0824 EMI requirement

2009/07  
 Modify

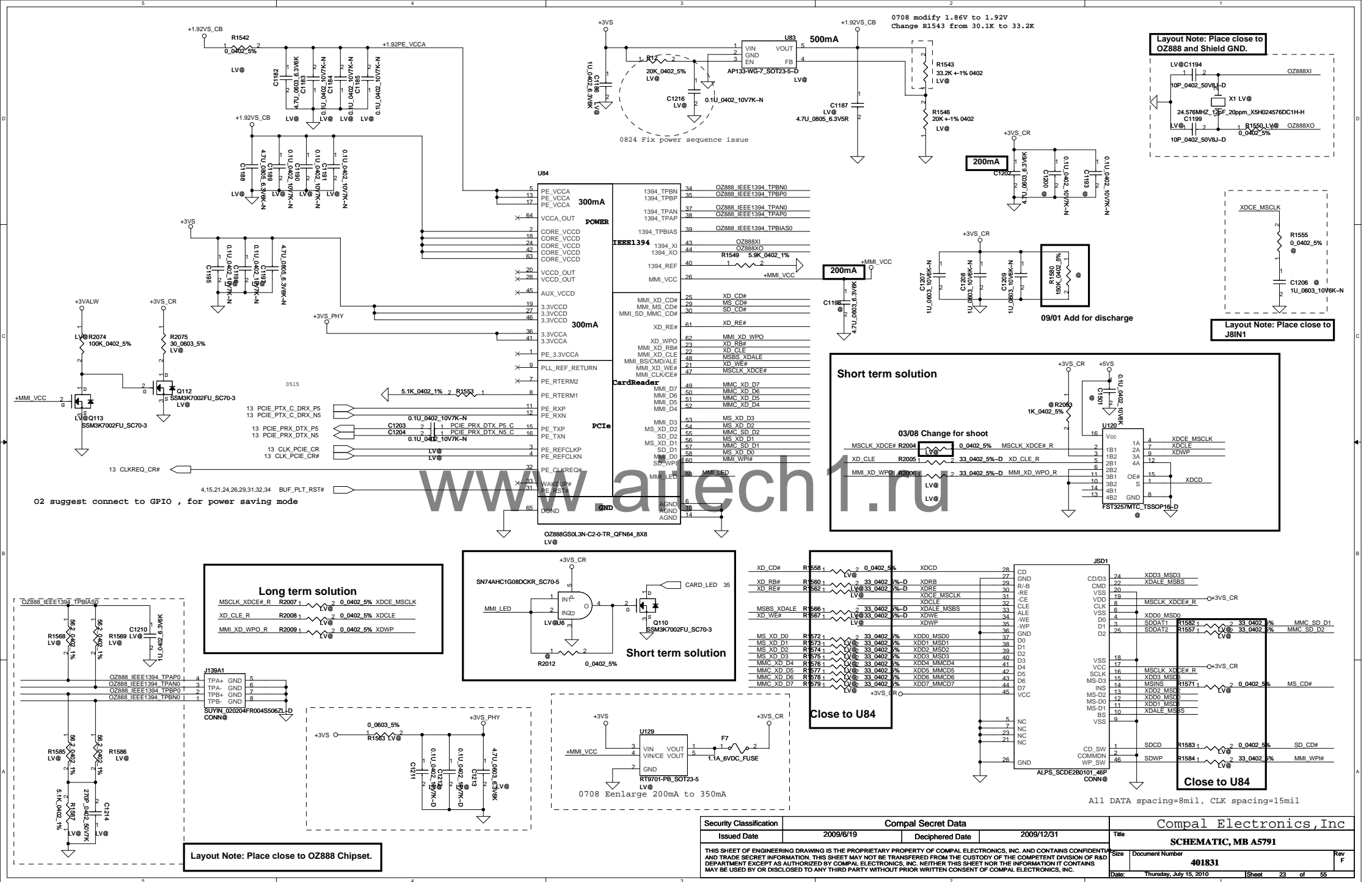
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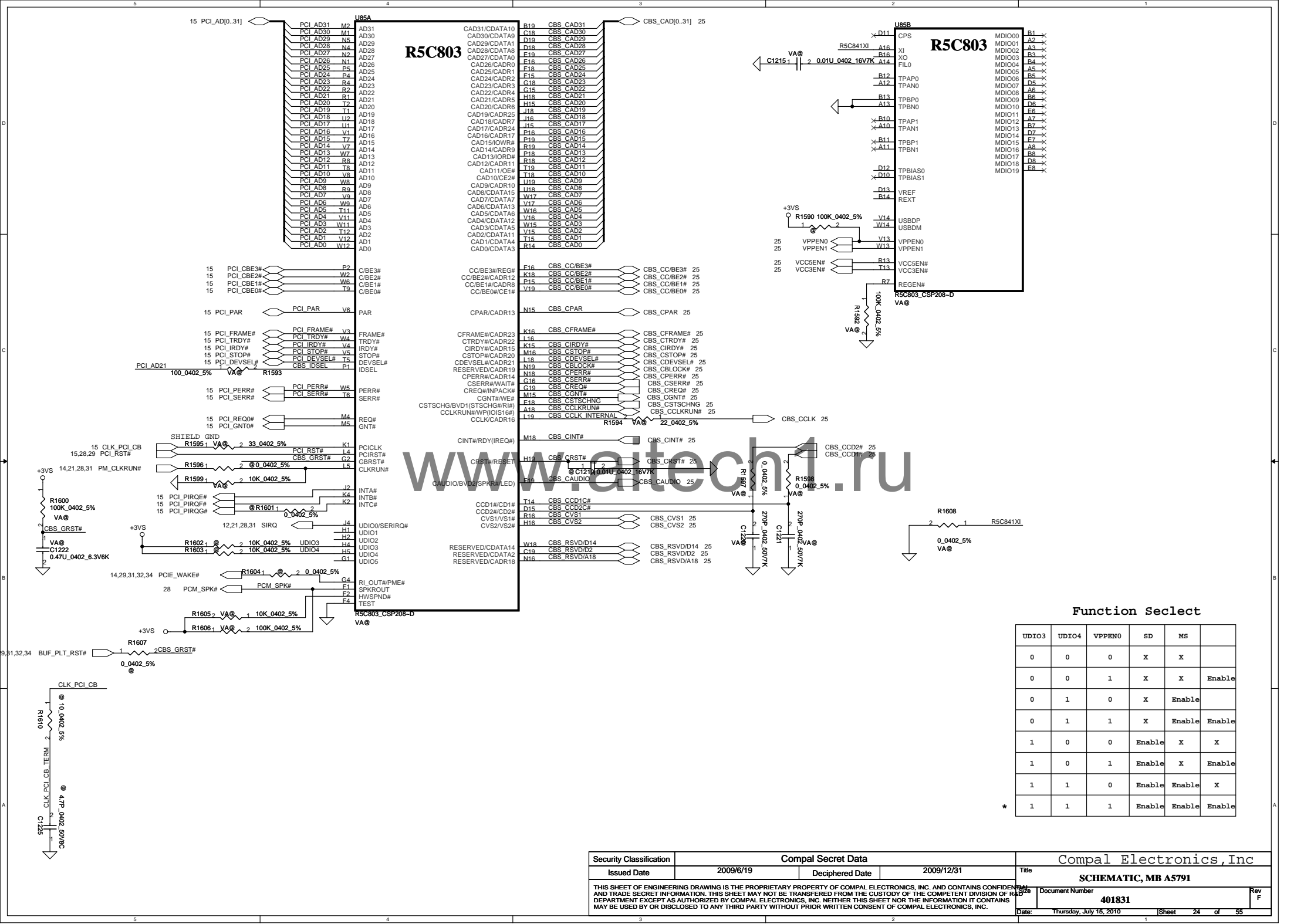
2009/07  
 Modify

07/10 Modify Q108 route

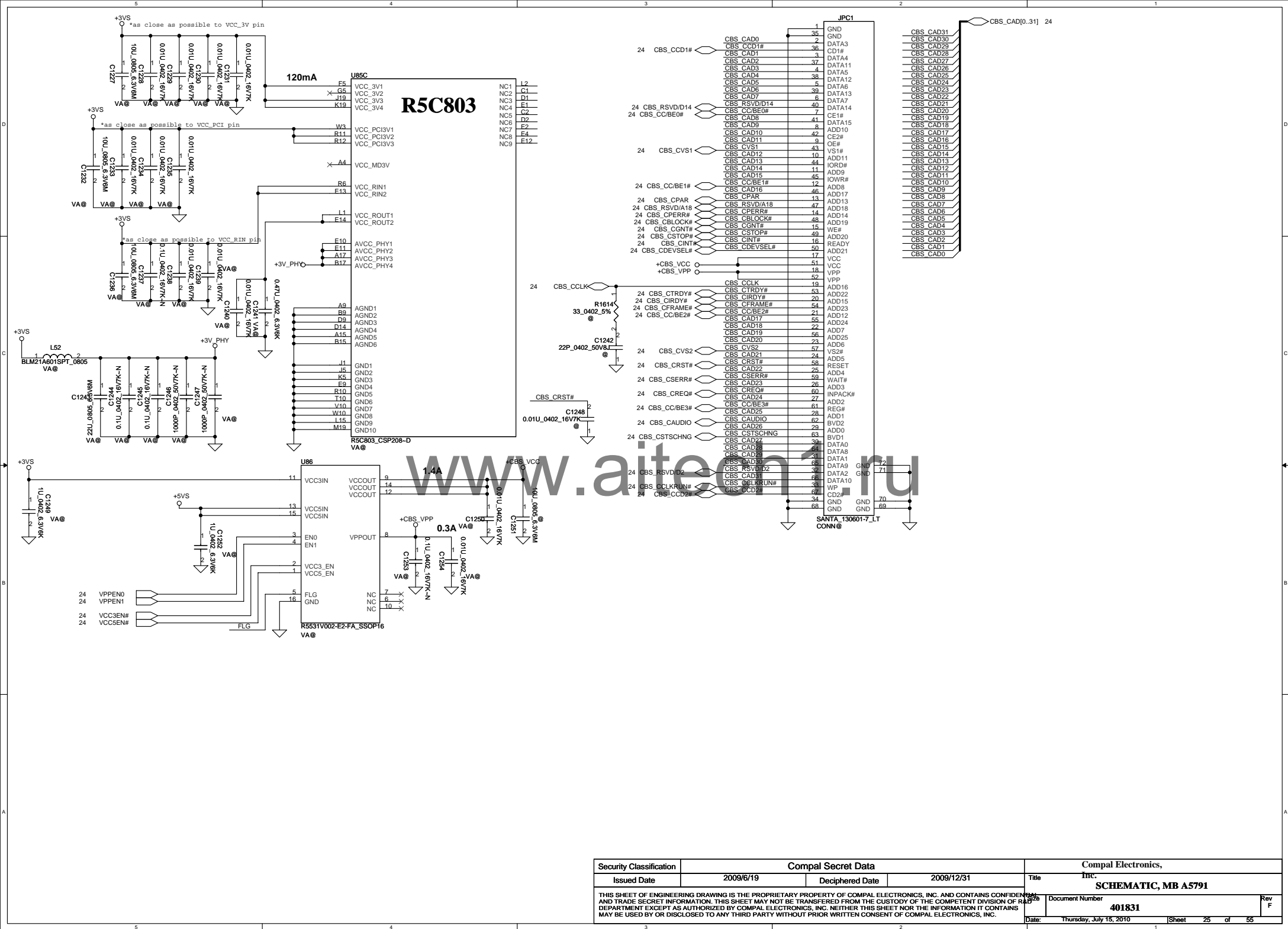
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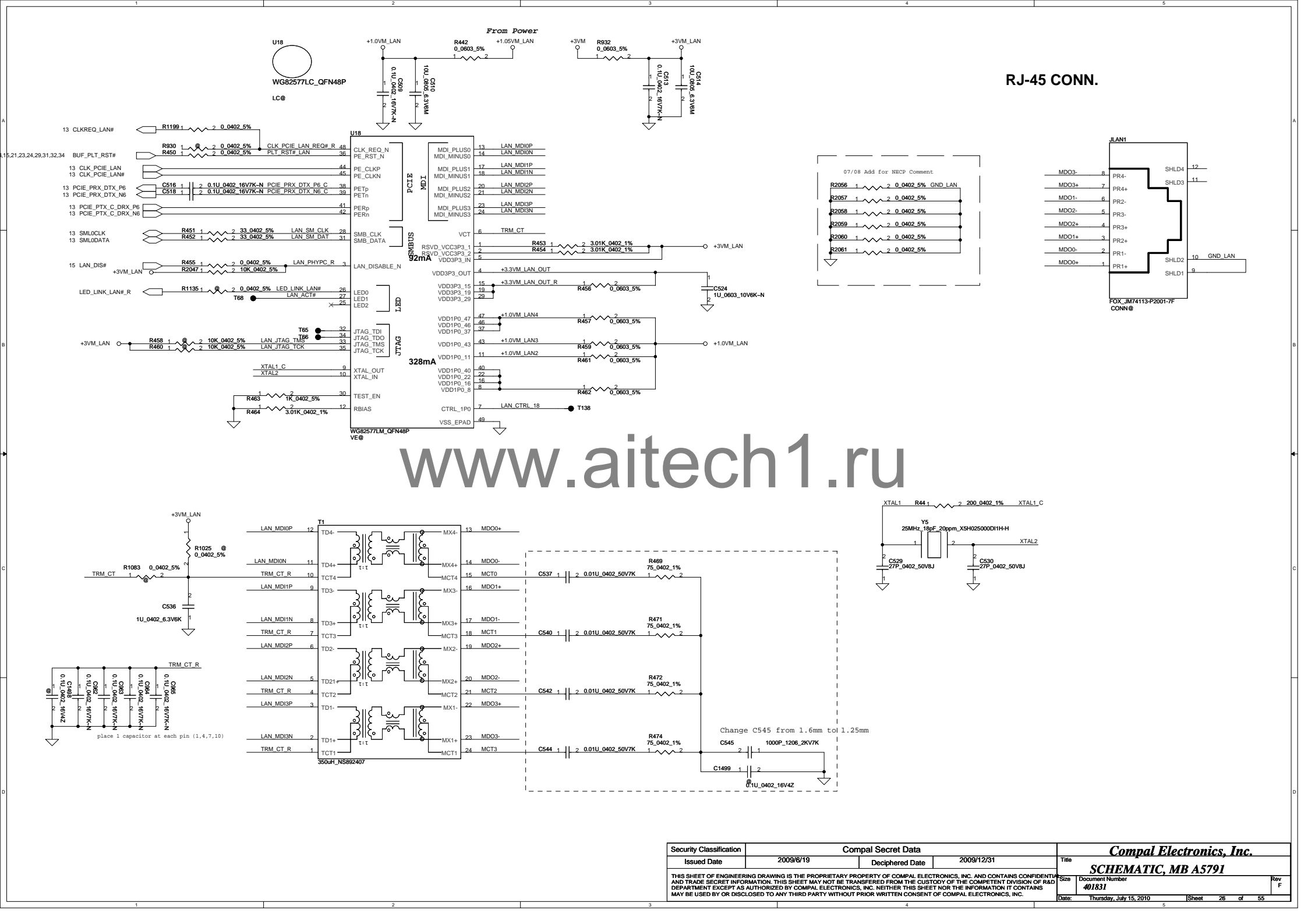


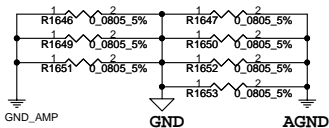
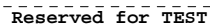
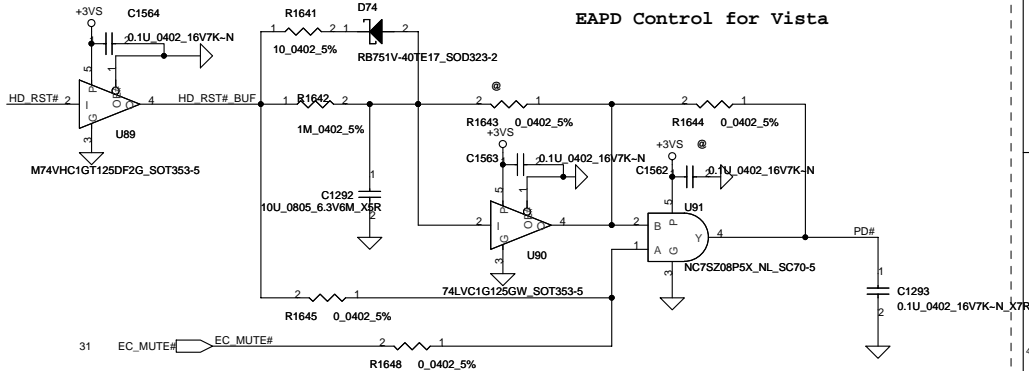
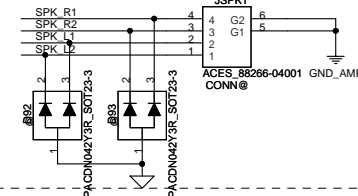
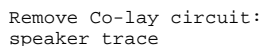






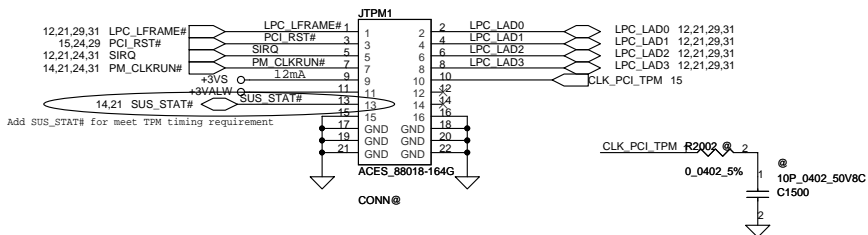
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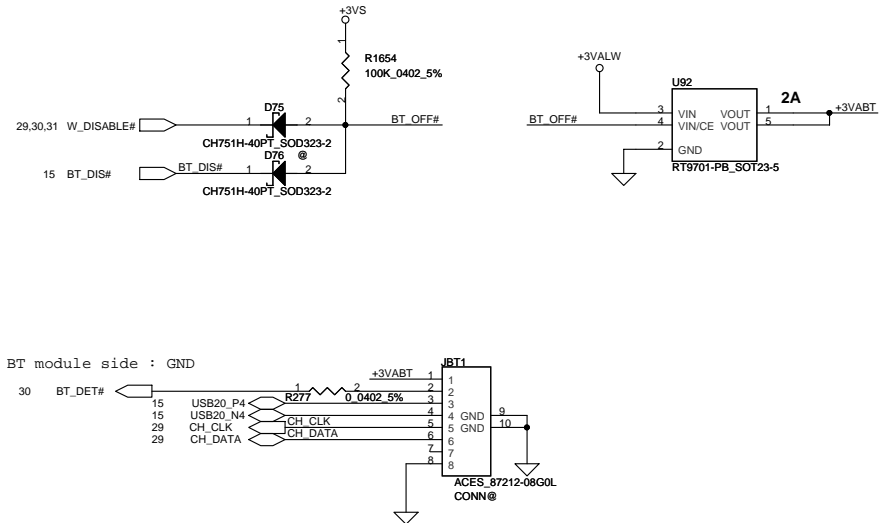


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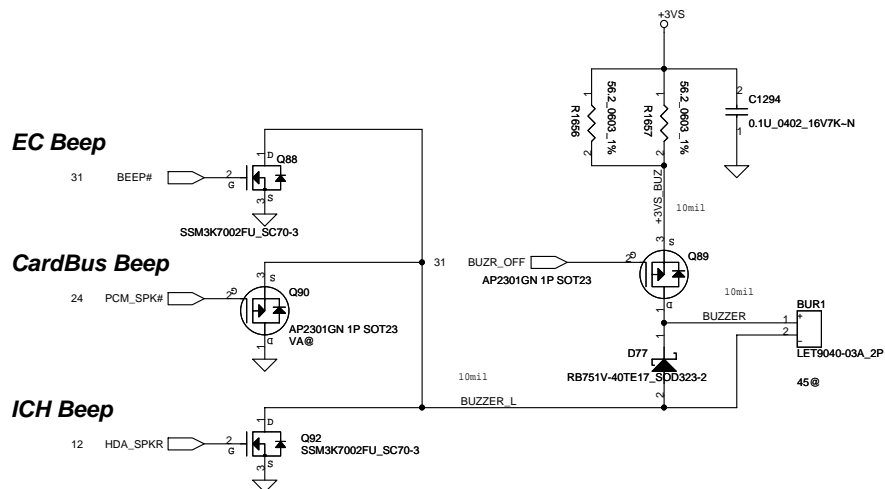
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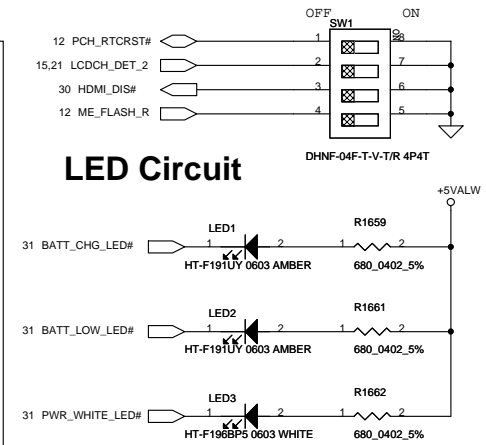
## Bluetooth



**BUZZER**



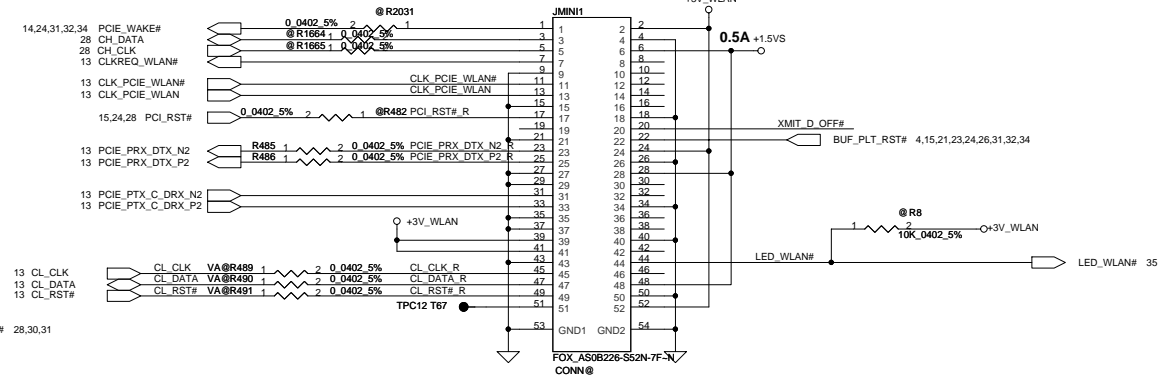
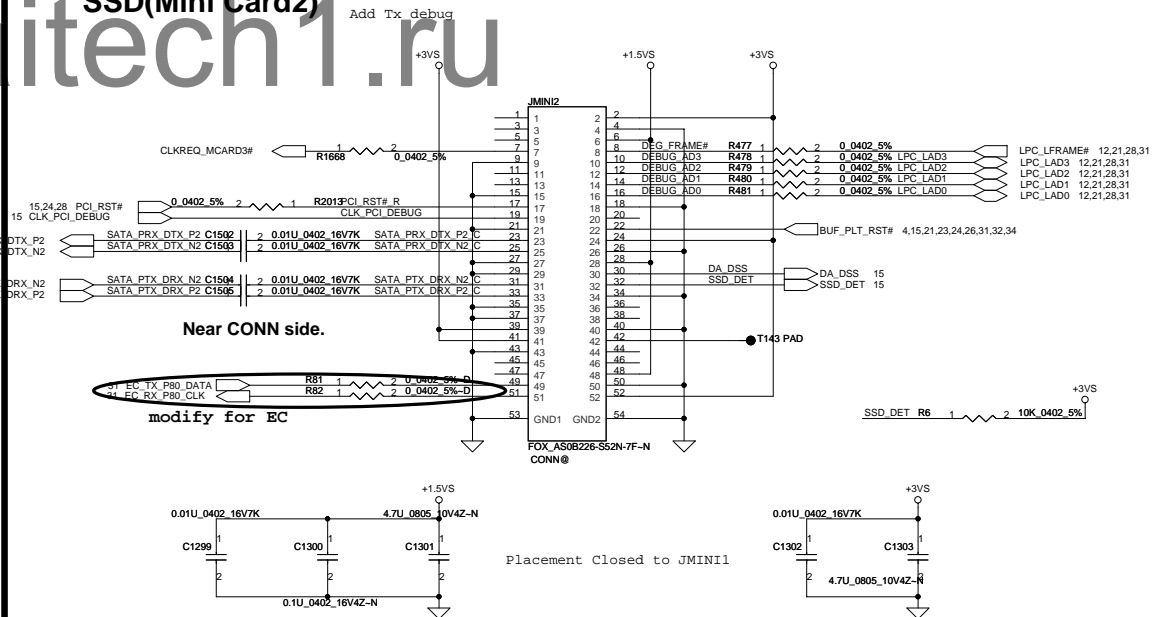
## LED Circuit



## 1208 Dimmer circuit

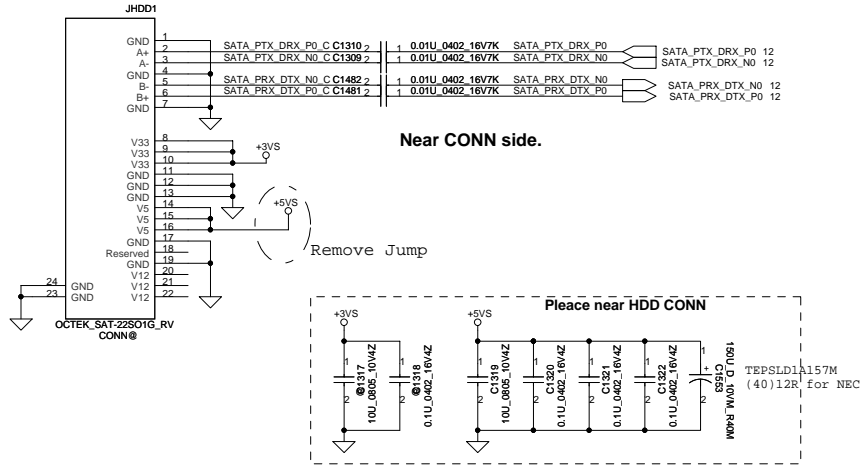
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Reserve for port80 card use for FCS in factory side. 10/17

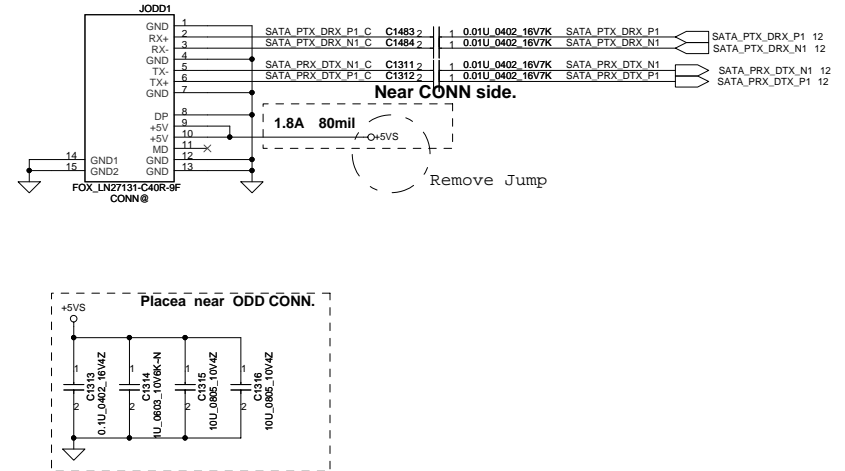
 $(+1.5V \Rightarrow 0.5A) \quad (+3V \Rightarrow 1A)$ 

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## SATA HDD CONN.



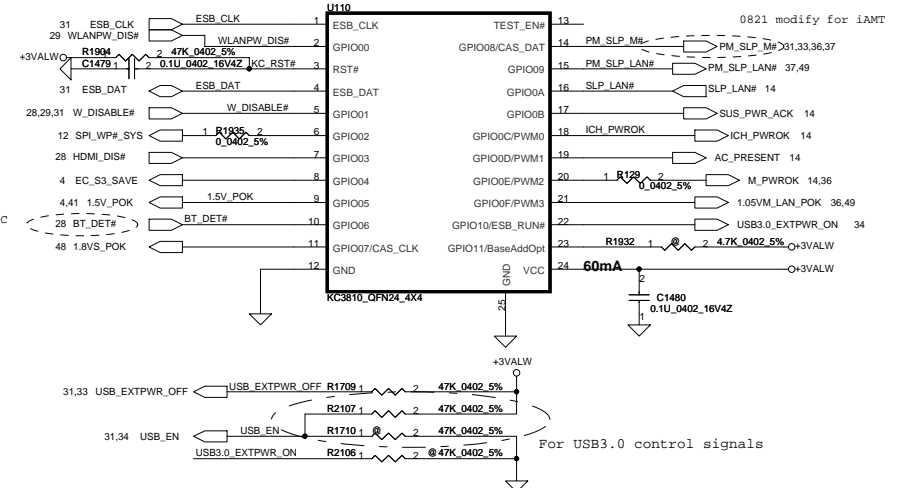
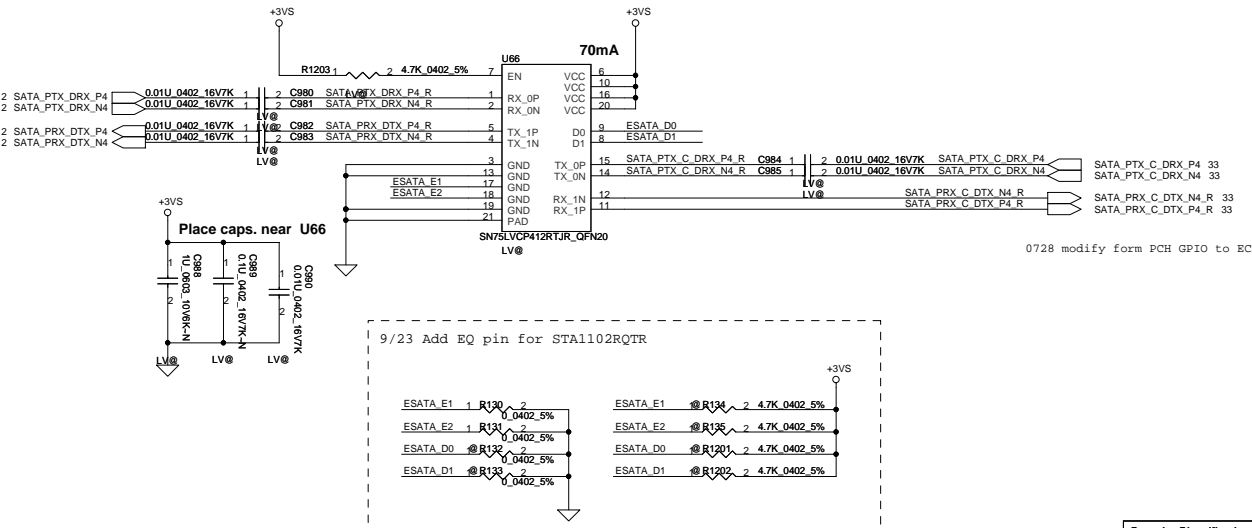
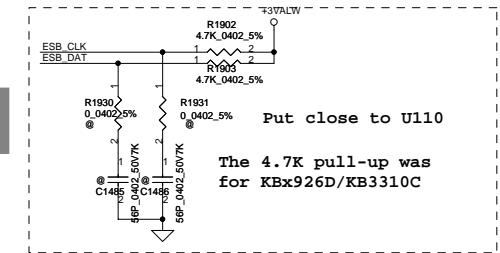
## SATA ODD CONN.



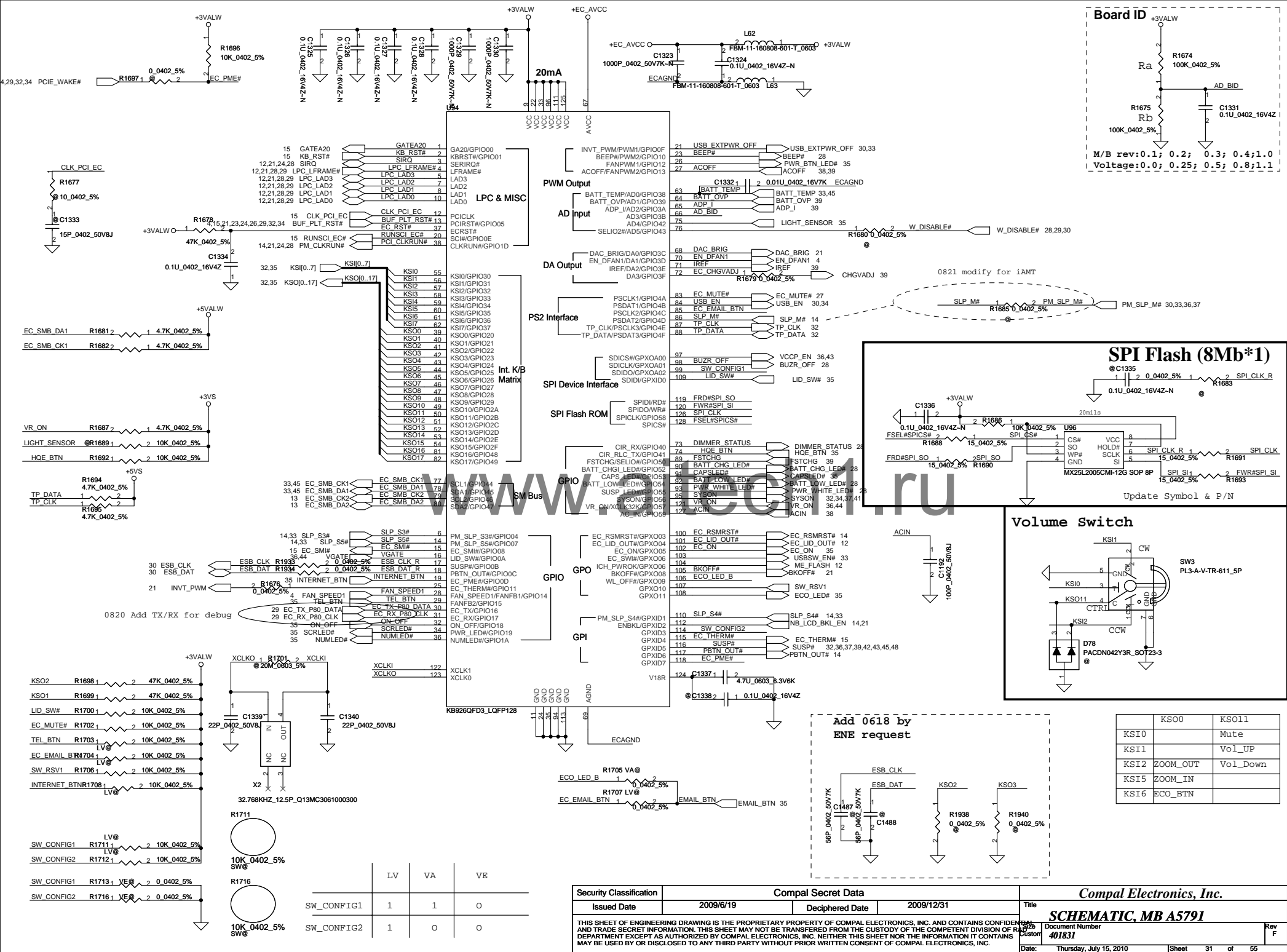
## E-SATA Redriver

www.aitech1.ru

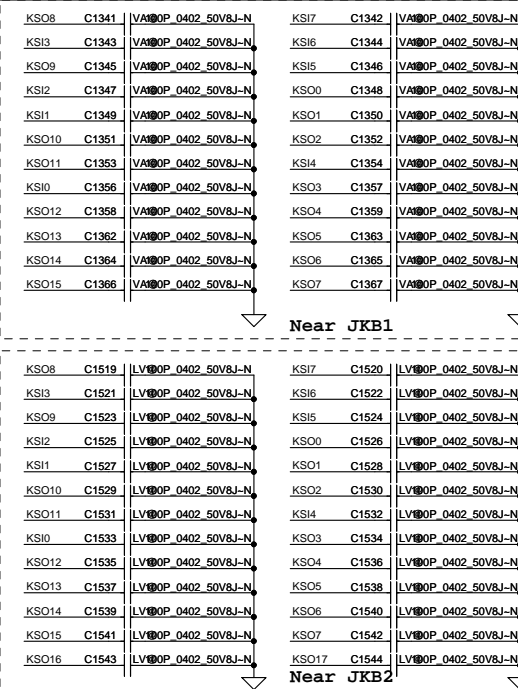
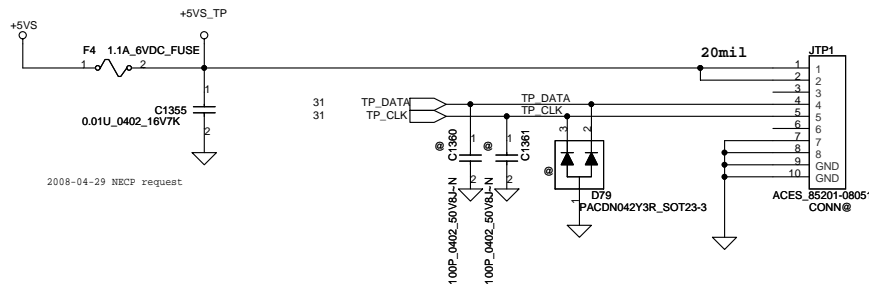
## EC3810



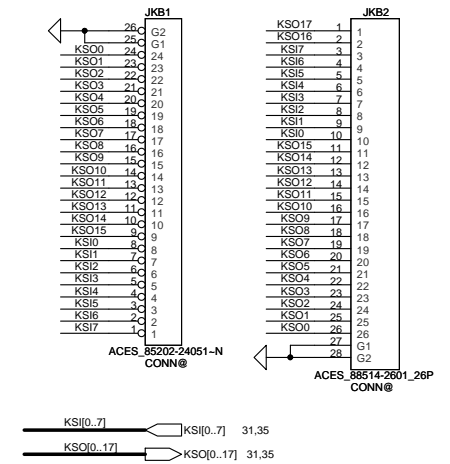
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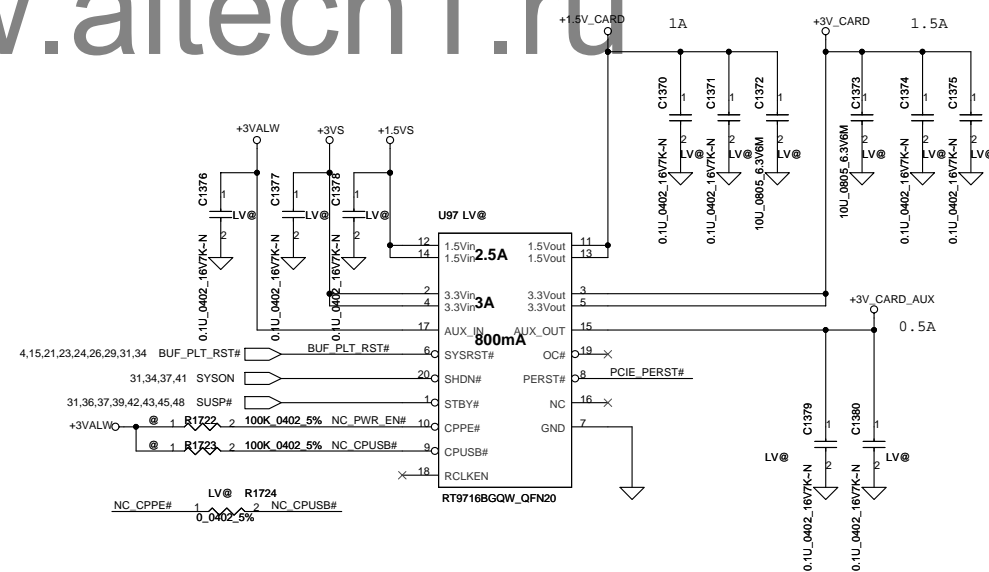
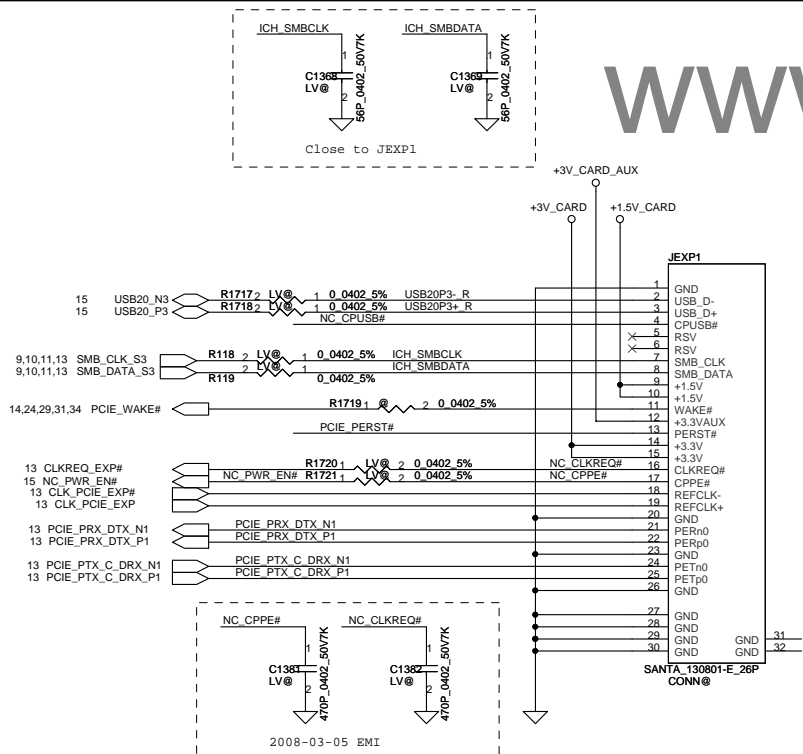
## TouchPad



**INT\_KBD CONN.**

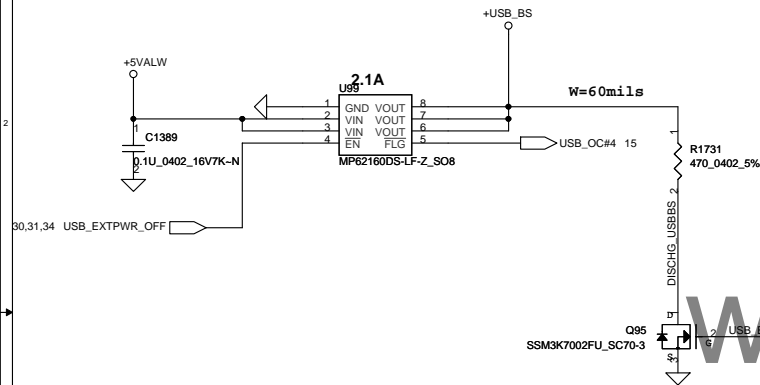
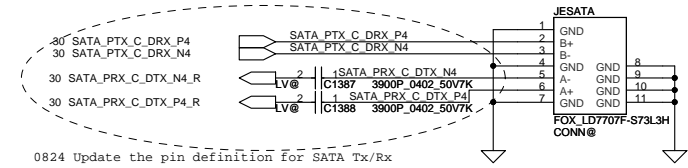
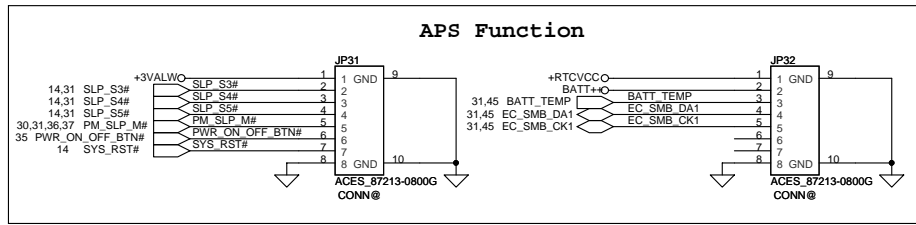


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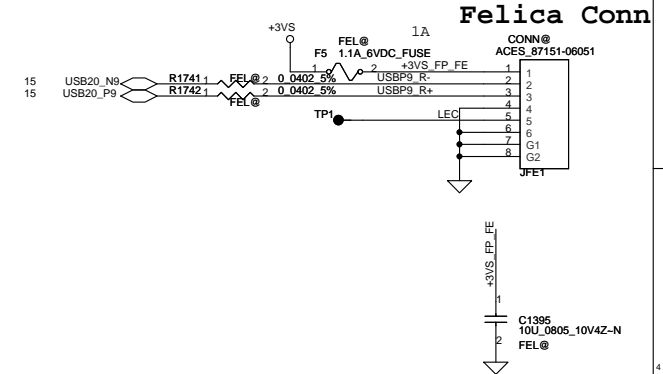
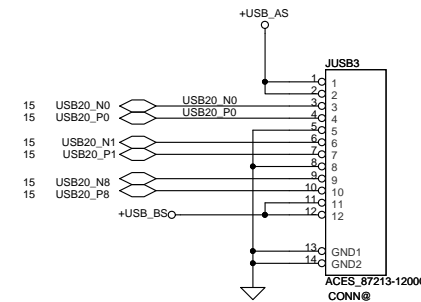
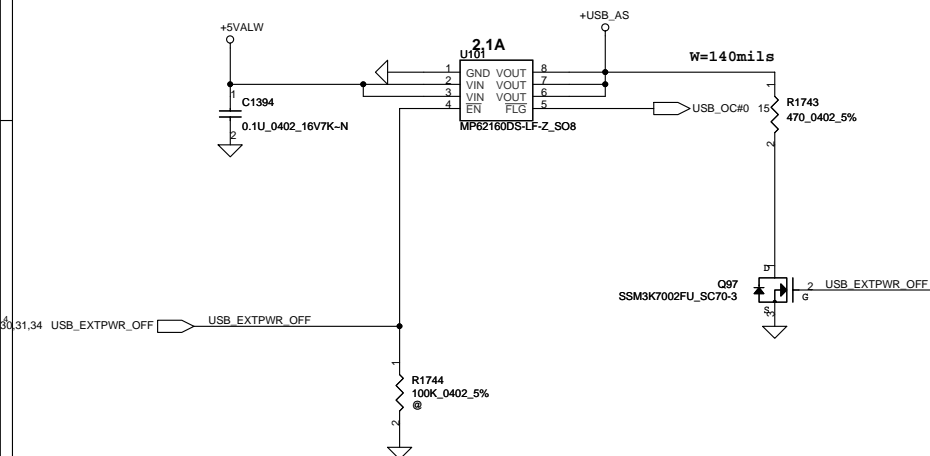


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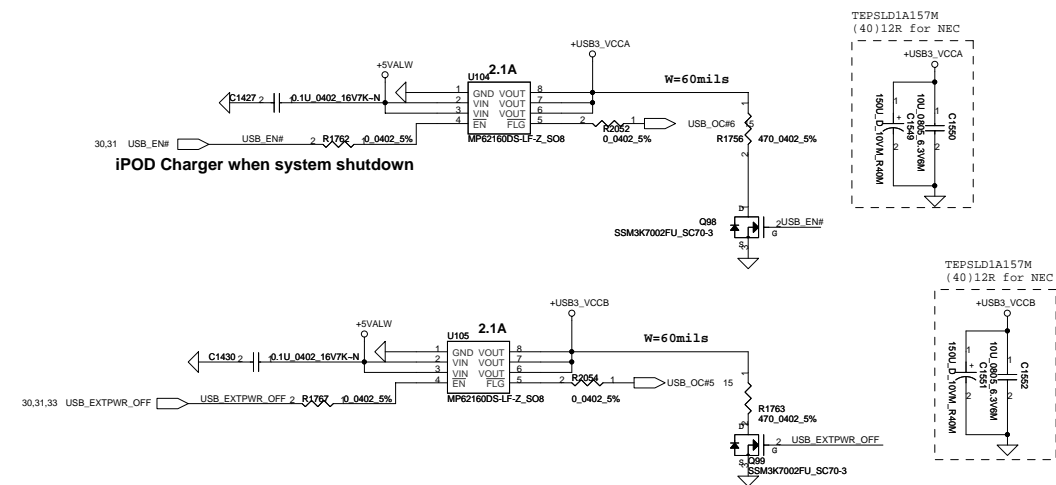
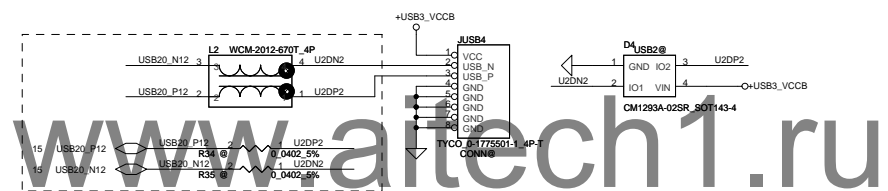
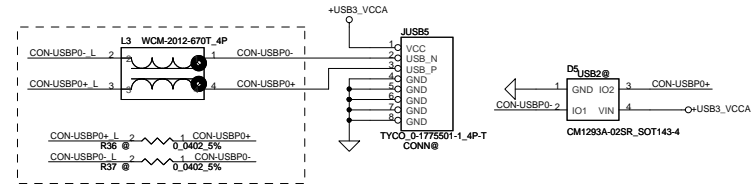
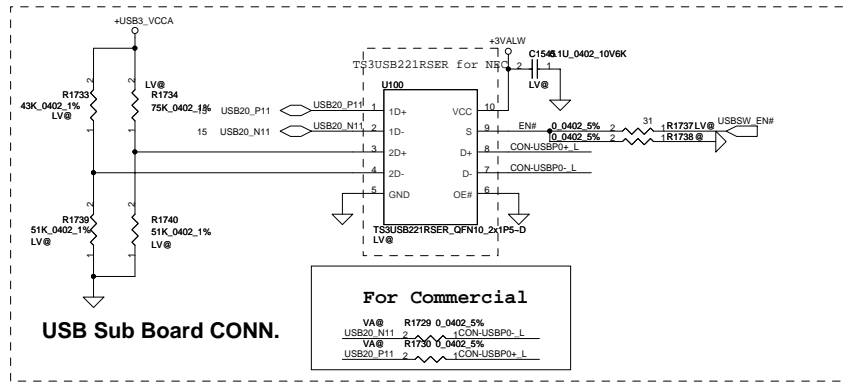




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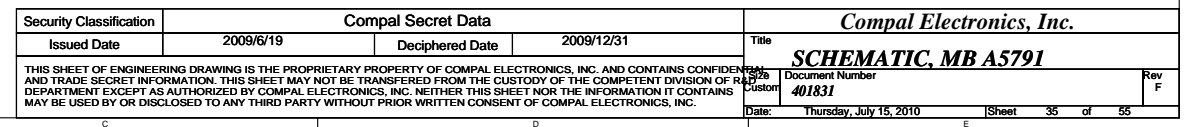
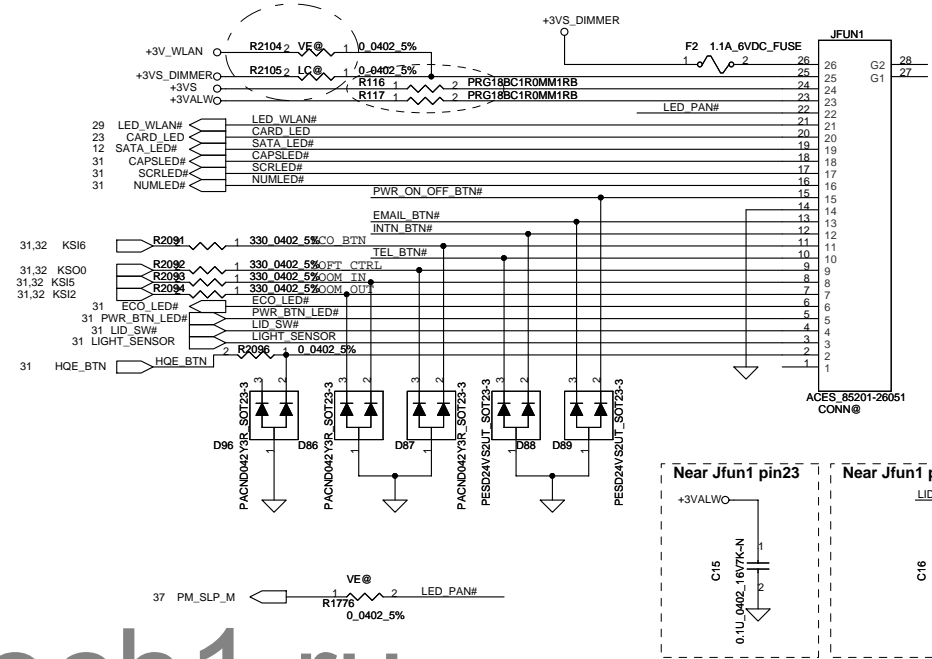


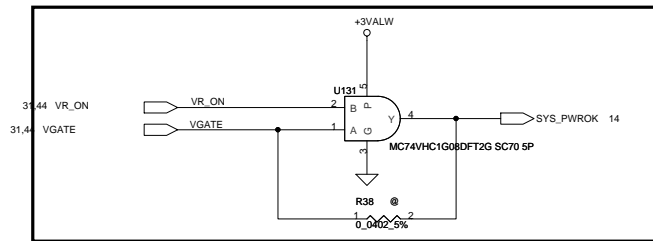
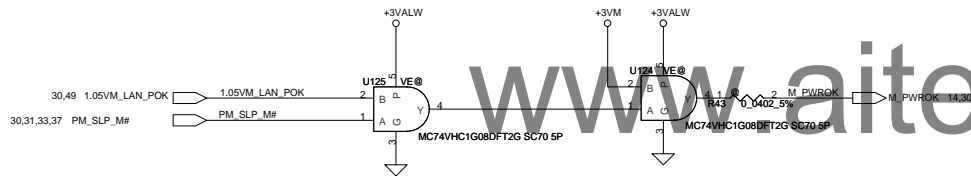
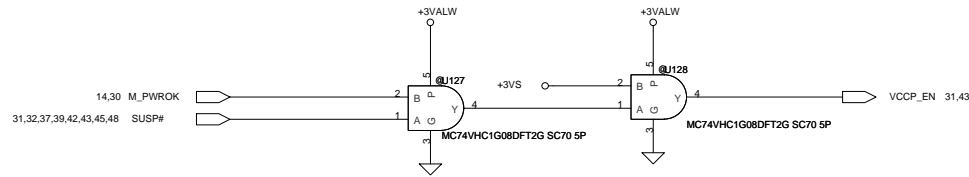
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USB\_EN Hi=Enable, Low=Disable IP0D USB power

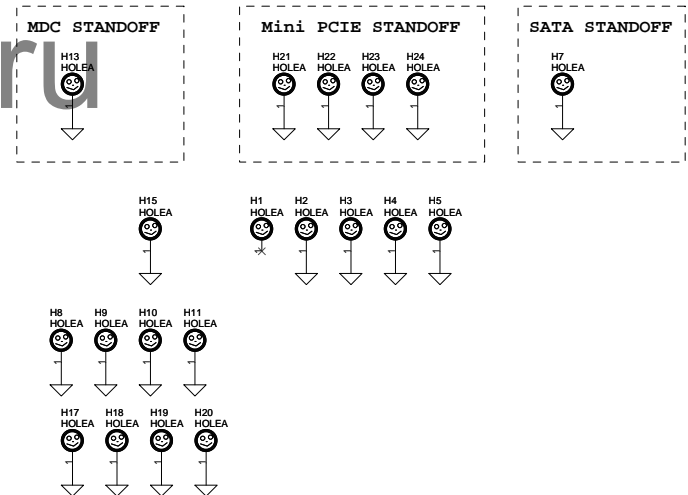
	BIOS MENU	S0	S3	S4	S5
AC	ON	ON	ON	ON	ON
DC	OFF	ON	OFF	OFF	OFF

**Function/B CONN.**



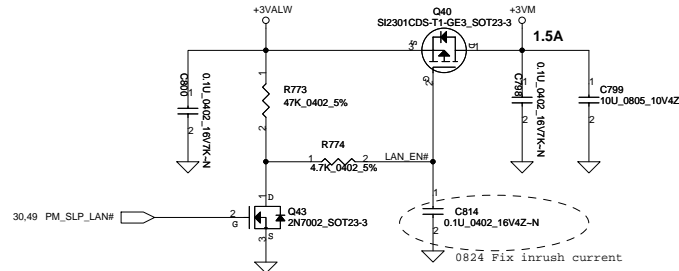
09/01 Add for tune vgate falling-time

Update Symbol

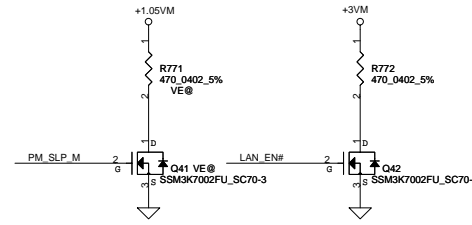


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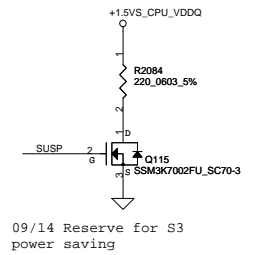
### +3VALW to +3VM Transfer



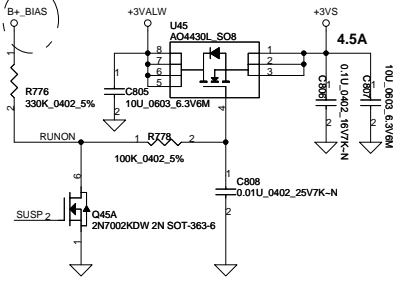
### Discharge circuit-2 for V-M



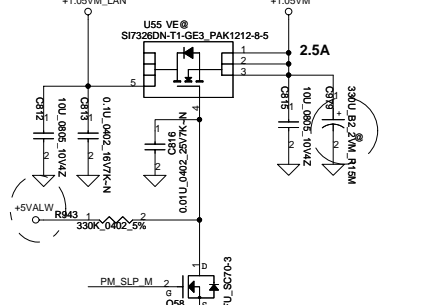
### +1.5VS\_VDDQ\_PP discharge



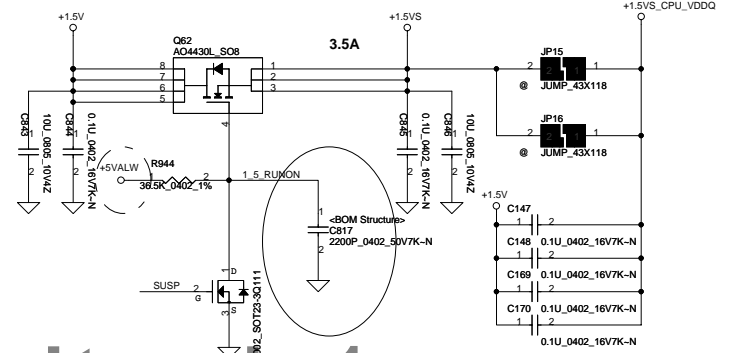
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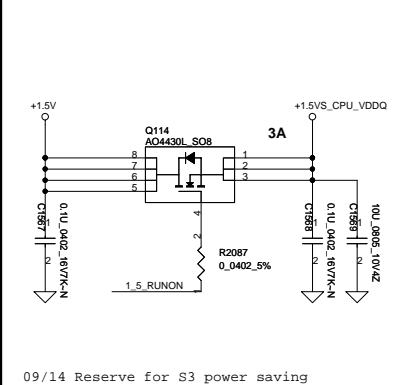
### +1.05VM\_LAN to +1.05VM Transfer



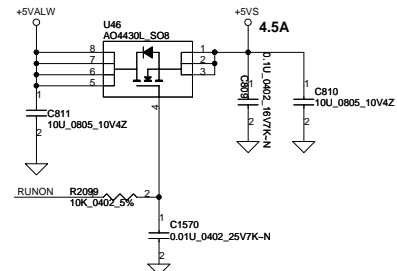
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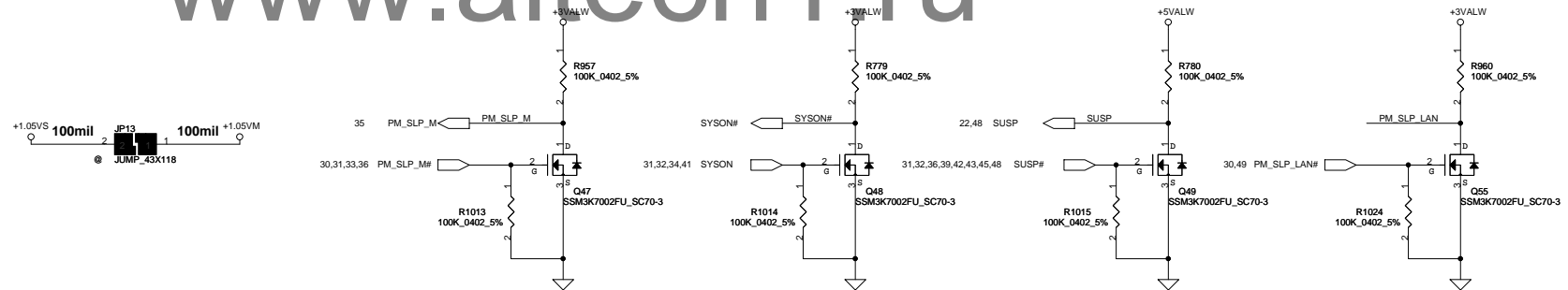
### +1.5V to +1.5VS\_VDDQ\_PP



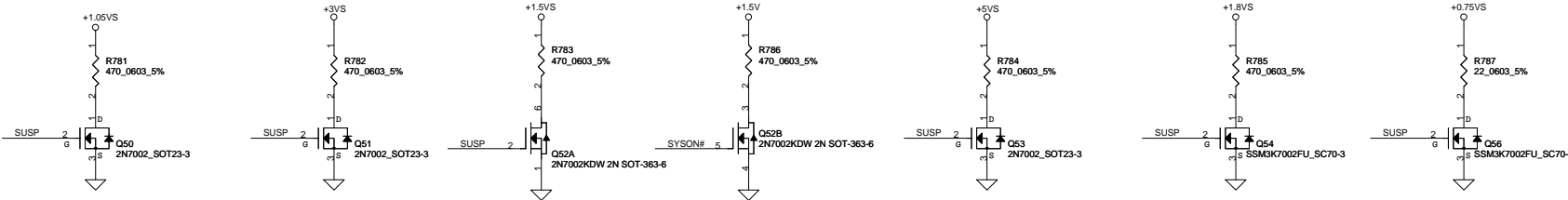
### +5VALW to +5VS Transfer



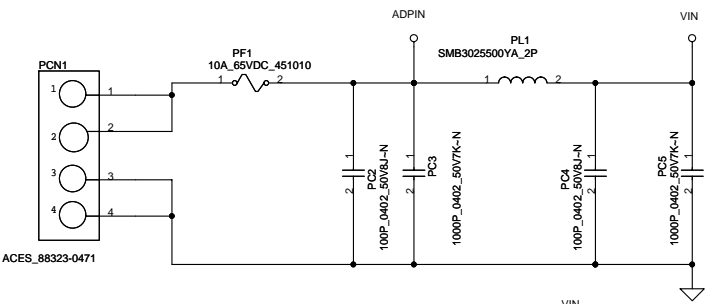
08/21Modify the Q58 for SMT



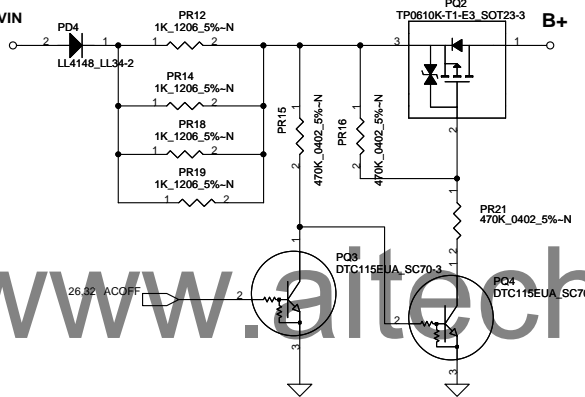
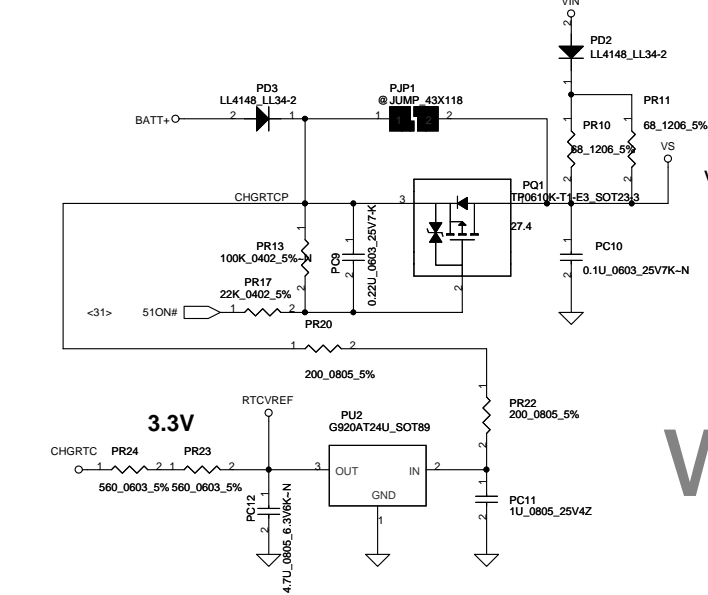
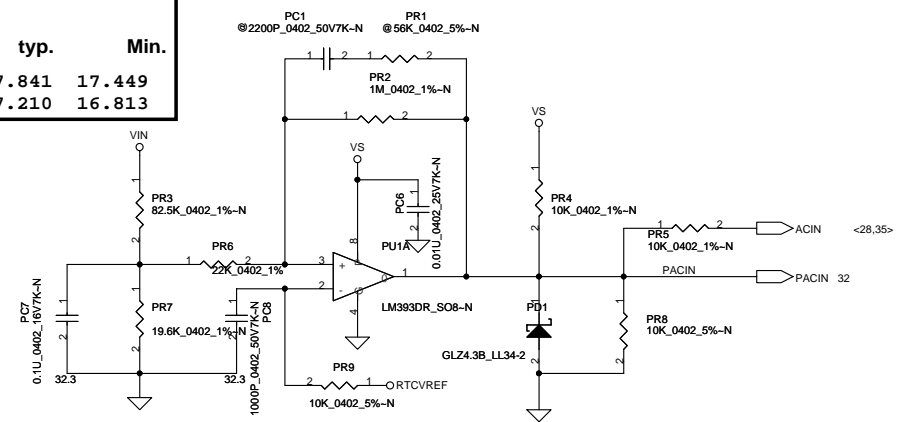
### Discharge circuit-1



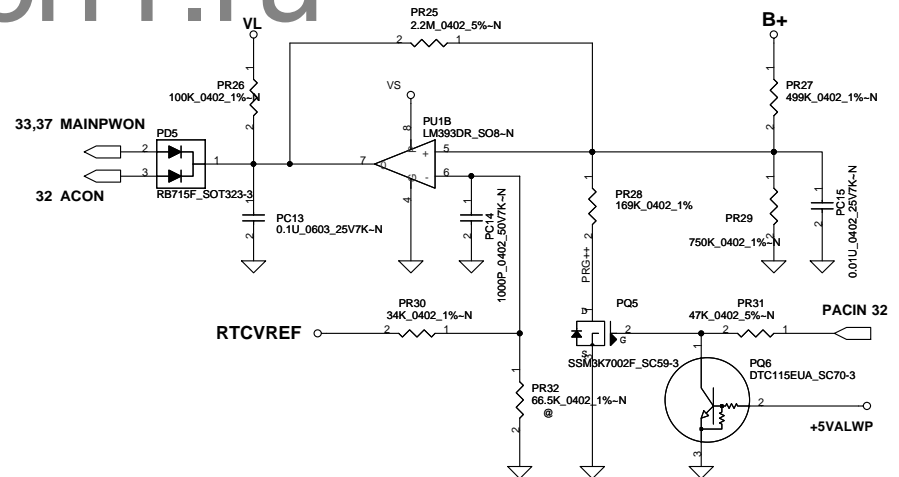
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Vin Detector			
	Max.	typ.	Min.
H-->L	18.234	17.841	17.449
L-->H	17.597	17.210	16.813

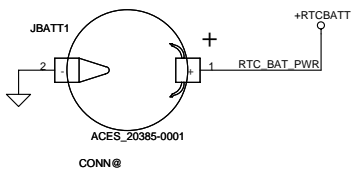


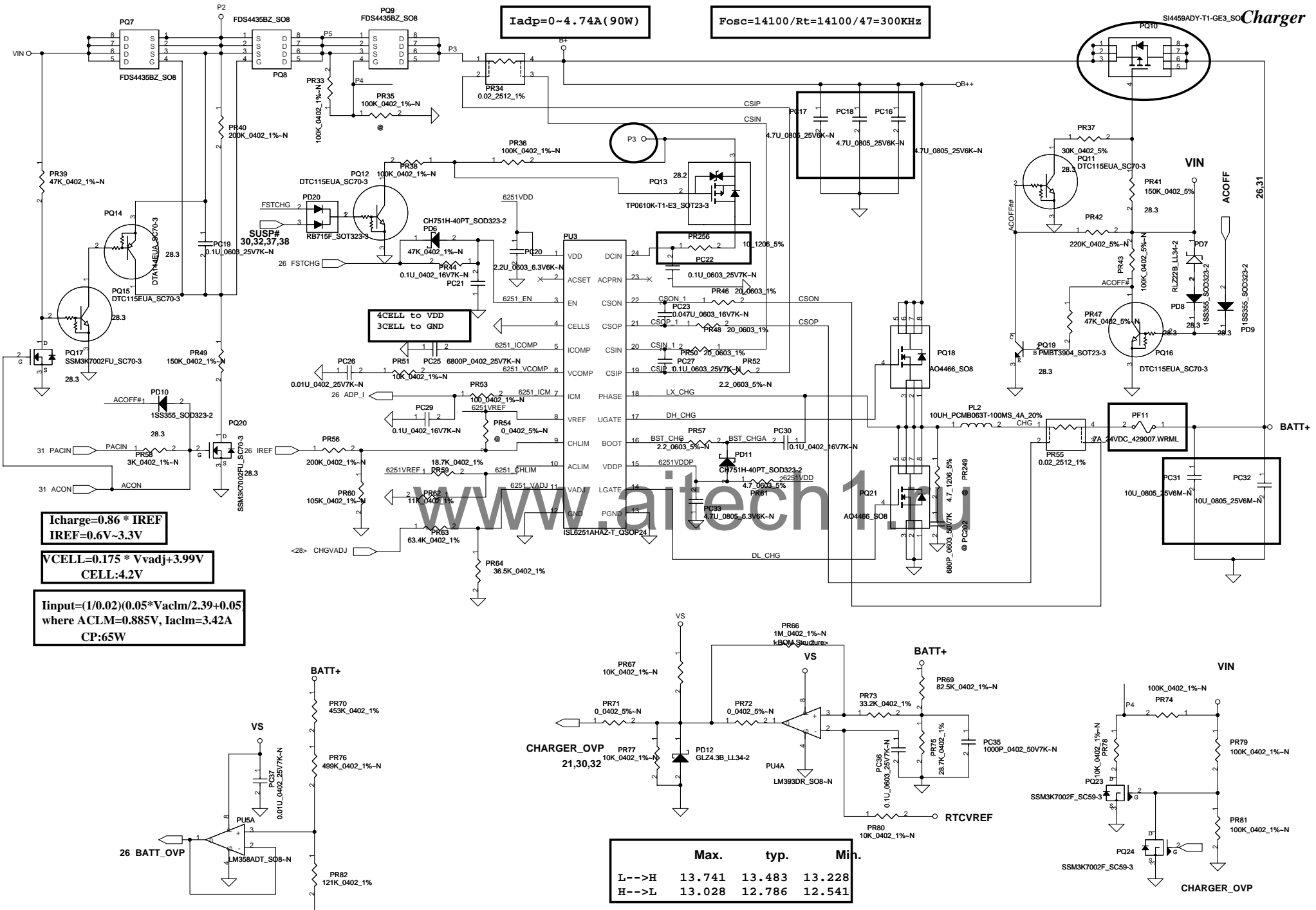
www.altech1.ru



ACIN			
Precharge detector			
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max
H-->L	4.92V	5.1V	5.25V
L-->H	6.062V	6.244V	6.43V



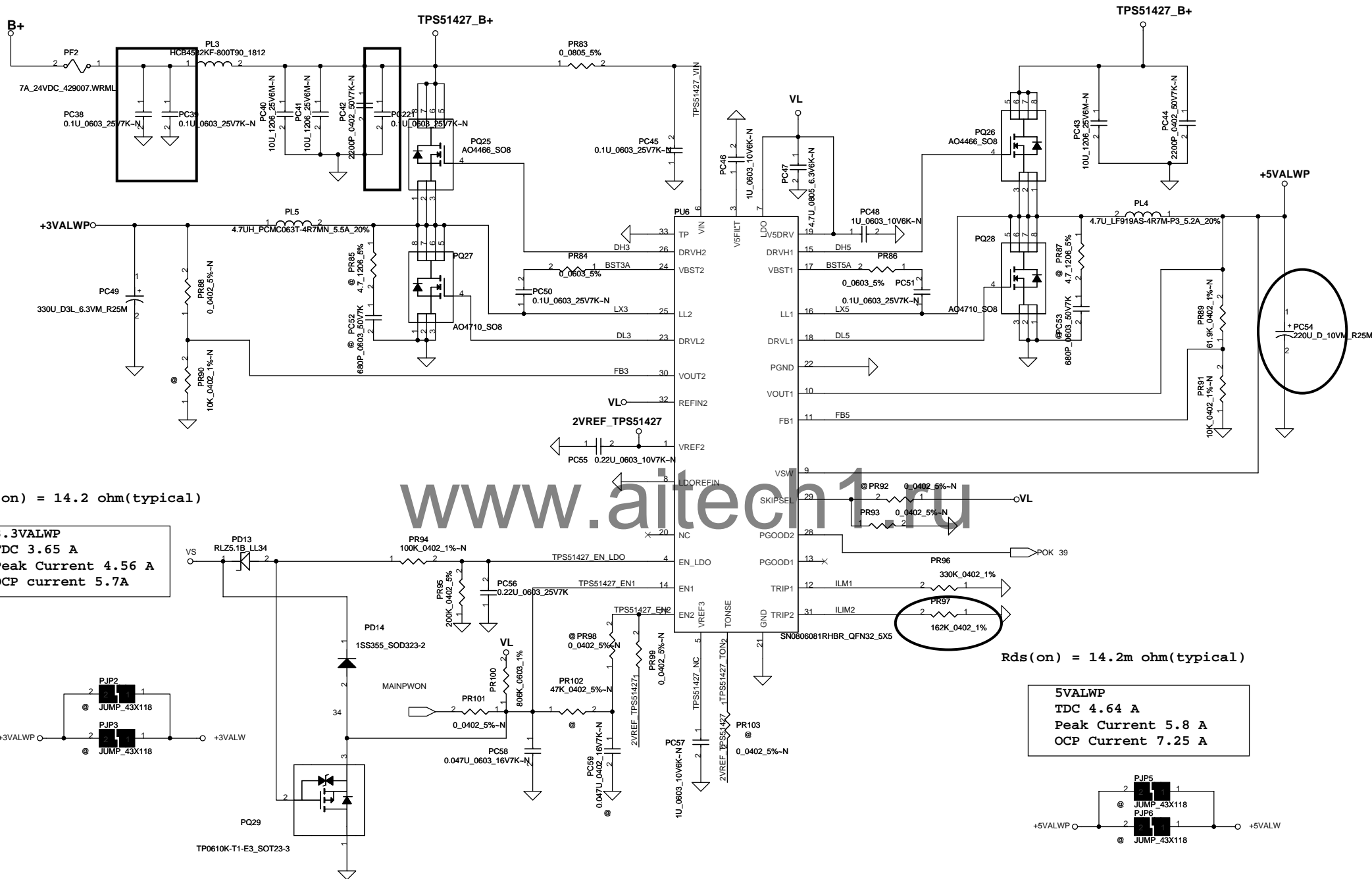


**I<sub>charge</sub>=0.86 \* I<sub>REF</sub>**  
**I<sub>REF</sub>=0.6V~3.3V**

**V<sub>CELL</sub>=0.175 \* V<sub>vadj</sub>+3.99V**  
**CELL:4.2V**

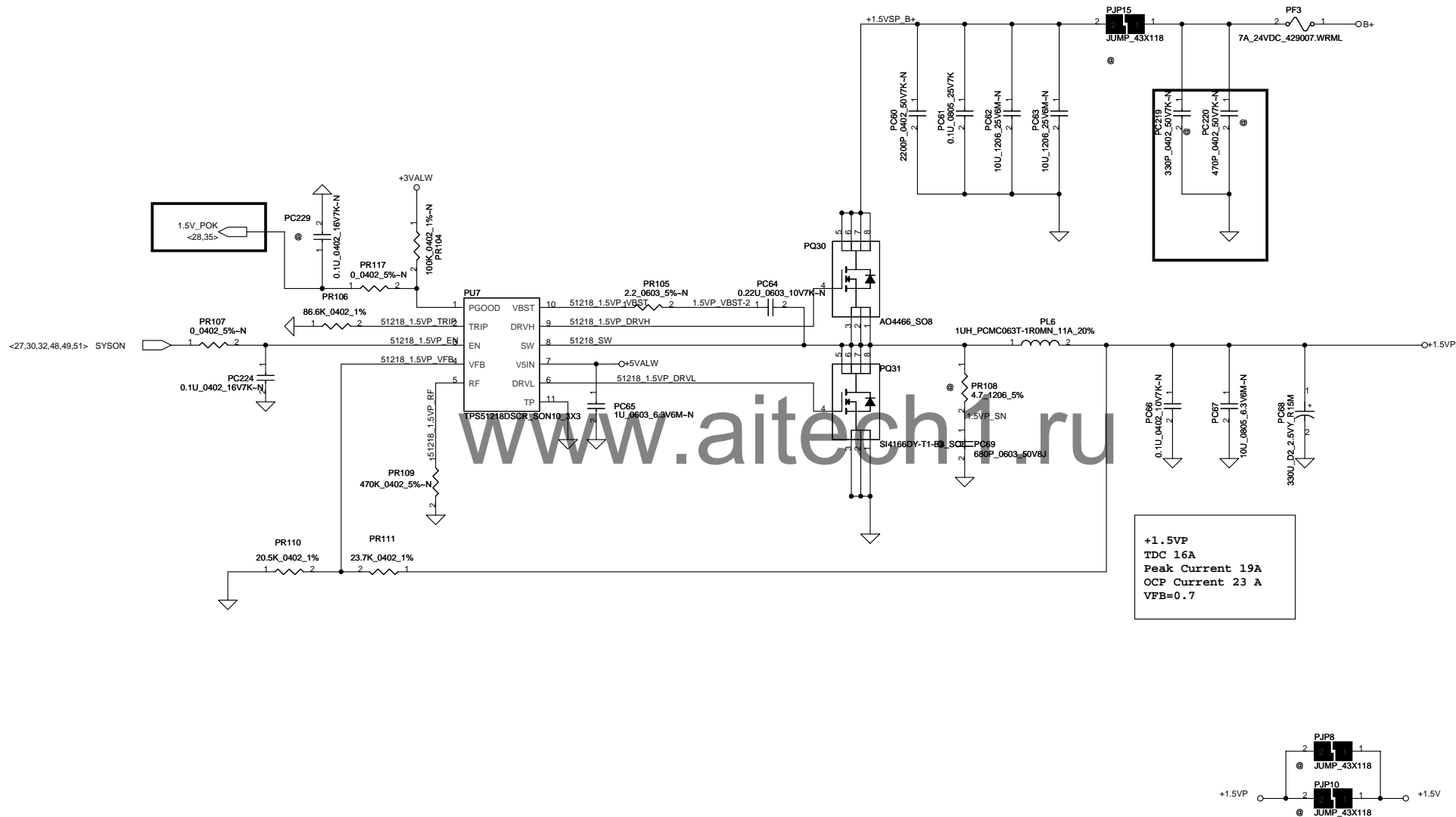
**I<sub>input</sub>=(1/0.02)(0.05\*V<sub>acm</sub>/2.39+0.05**  
**where ACLM=0.885V, I<sub>acm</sub>=3.42A**  
**CP:65W**

	Max.	typ.	Min.
L-->H	13.741	13.483	13.228
H-->L	13.028	12.786	12.541

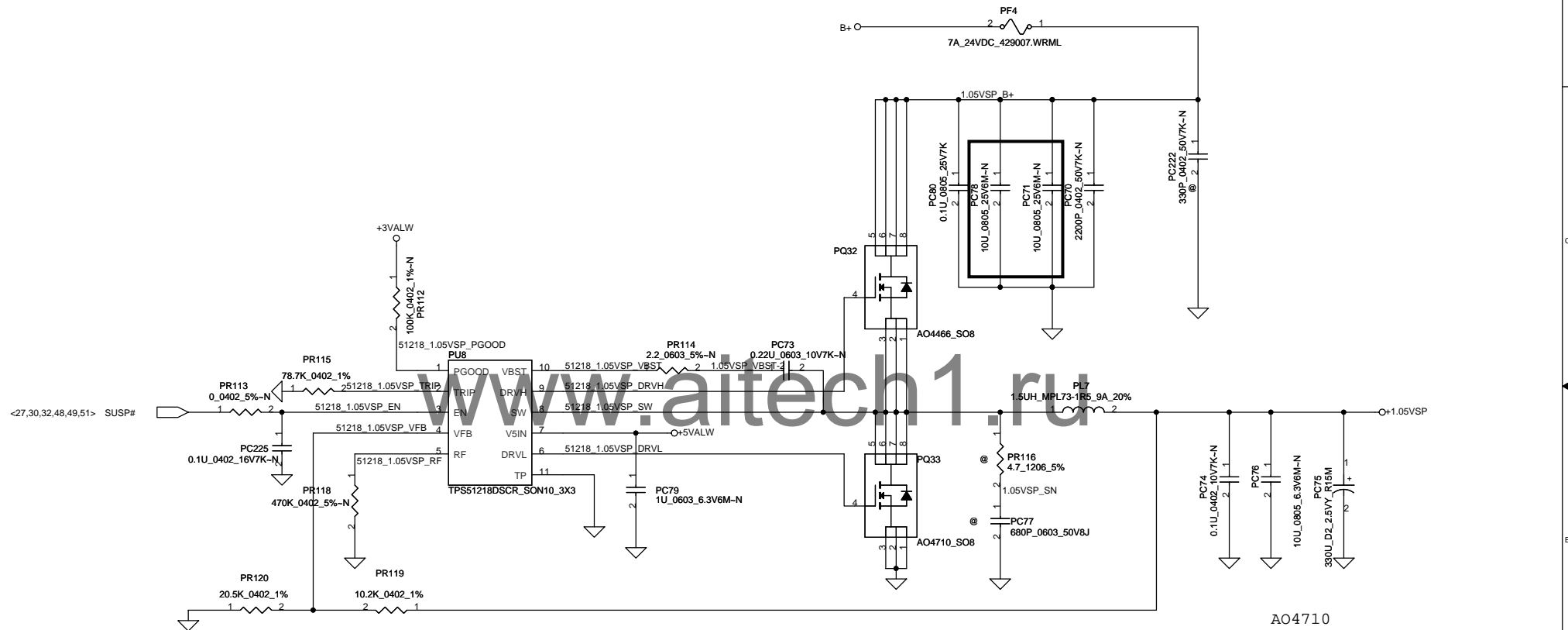


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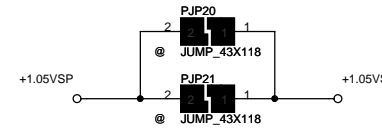
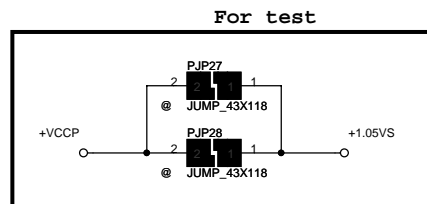




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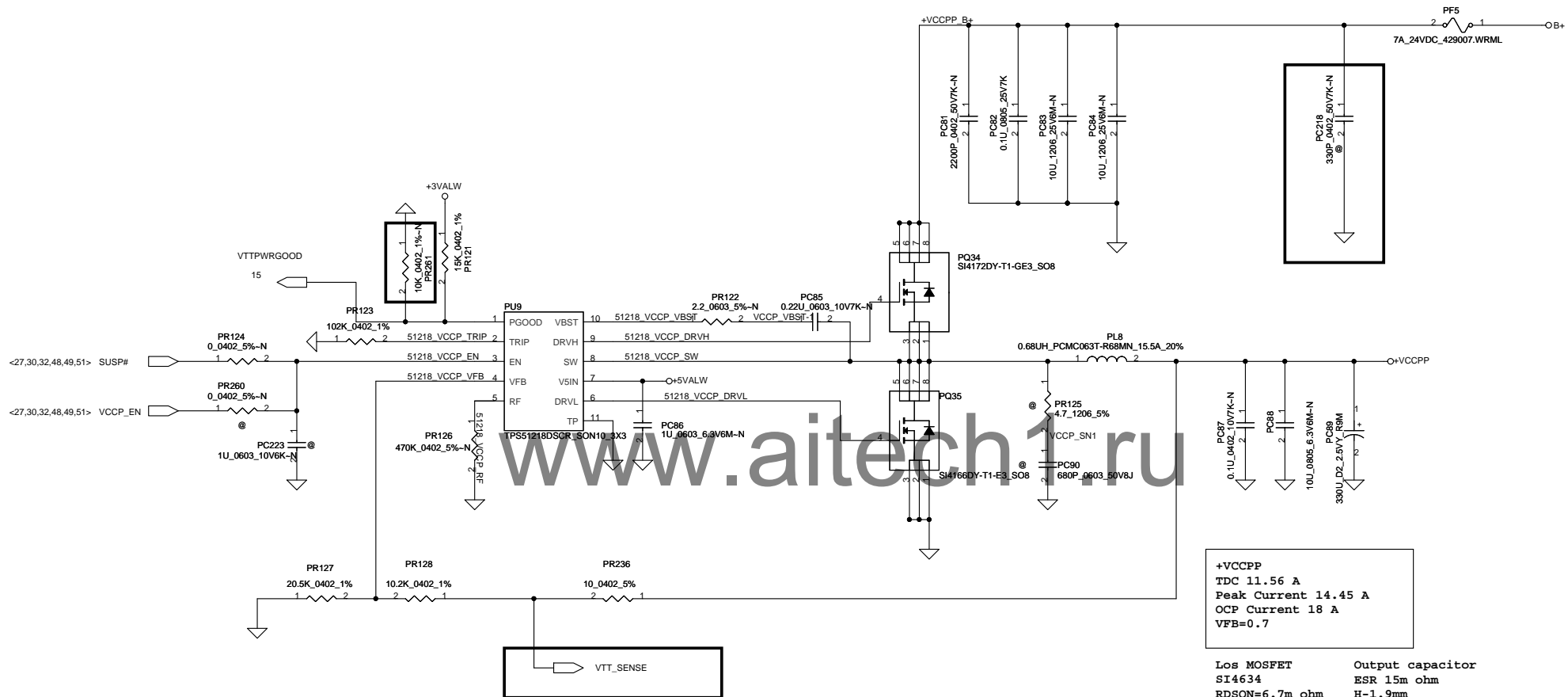


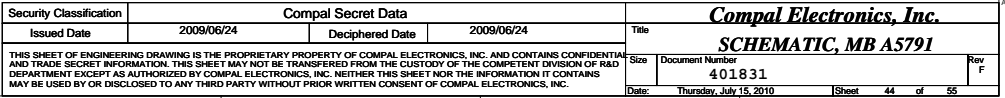
AO4710  
Rds(on)=14.2 mohm  
+1.05VSP  
TDC 4.37A  
Peak Current 5.46 A  
OCP Current 6.83 A



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+VCCPP



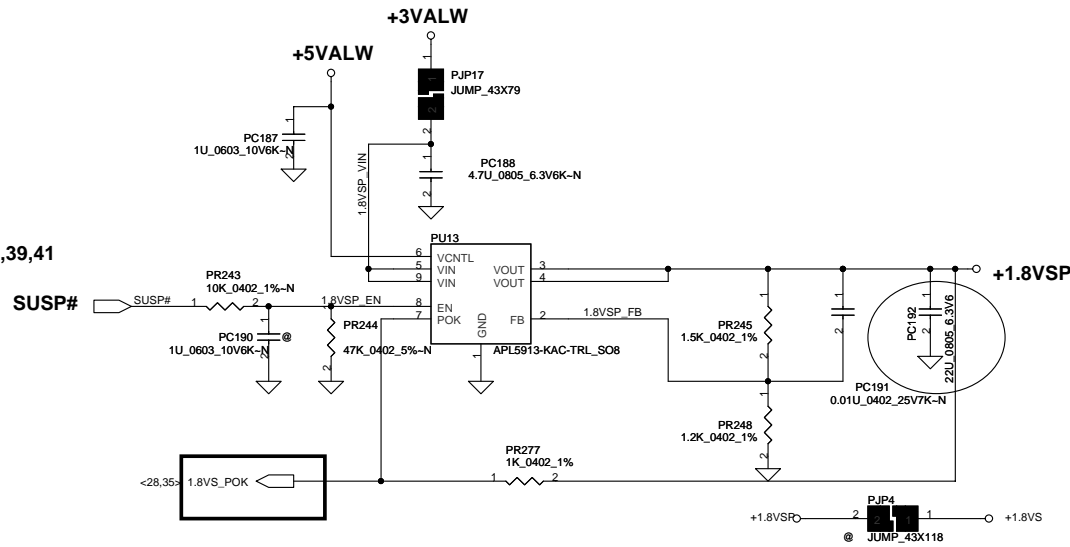




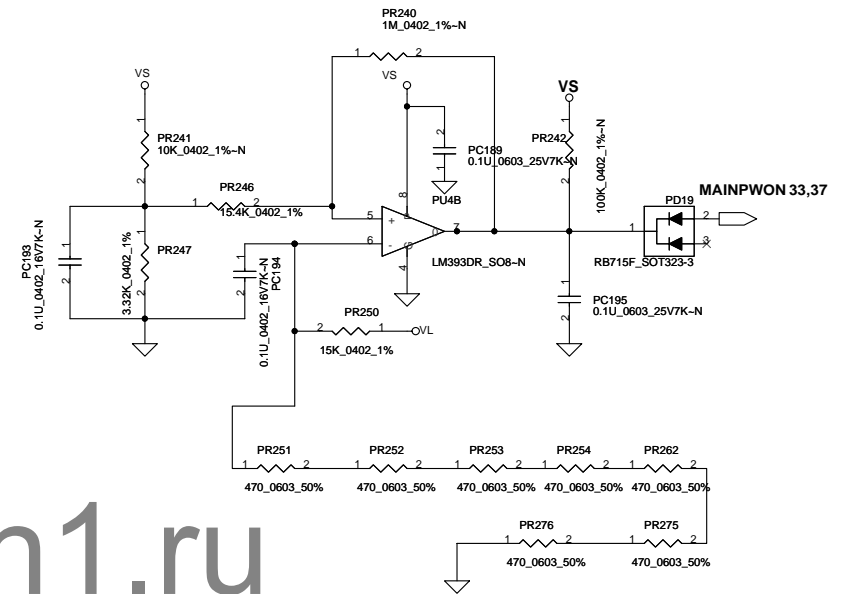




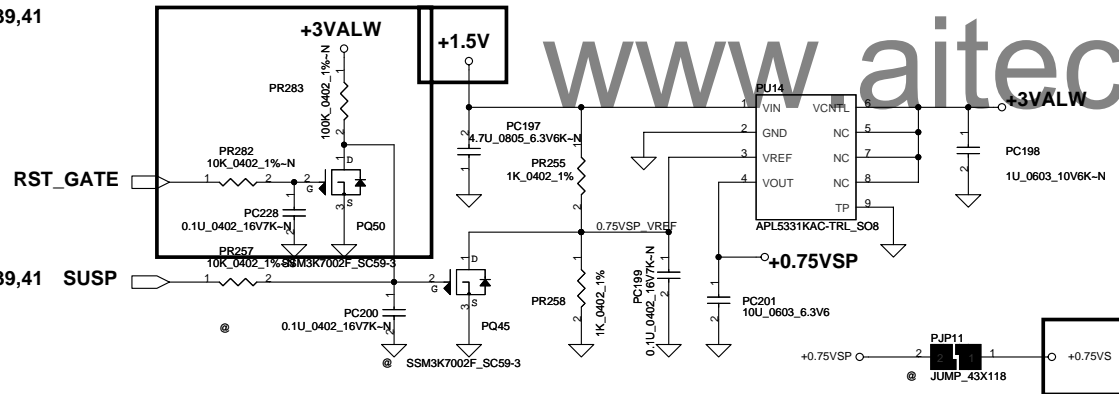
27,28,30,34,39,41



Posestos



27,28,30,34,39,41



27,28,30,34,39,41

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Schematic	Rev.
1	44	PWR-CPU_CORE	2009/08/04	COMPAL	Change the CPU current gaing meet Arrandale CPU	DEL(SD028100180 S RES 1/16W 1K +-5% 0402) Location :PR135 PR140 ADD(SD028100180 S RES 1/16W 1K +-5% 0402) Location :PR136 PR139		0.1
2	44	PWR-CPU_CORE	2009/08/04	COMPAL	Change the resiter value to same with common circuitry	Change (SD028470280 S RES 1/16W 47K +-5% 0402) to (SD000009080 S RES 1/16W 1.91K +-1% 0402) Location :PR146		
3	41~49	PWR-1.5VP, 1.05VSP, VCCPP, 1.05VM	2009/08/04	COMPAL	Change the output capacity to same with common circuitry	Change (SGN00000500 S NBO CAP 330U 2.5V M Y NO H2.0) to (SGA19331360 S POLY C 330U 6.3V M D3L ESR25M TPE H2.8 ) Location :PC68 PC75 PC89 PC211		
4	39	PWR-Charger	2009/08/04	COMPAL	Change the schematic to same with common circuitry	Change (SB000009610 S TR SSM3K7002FU 1N SC70-3) to (SB301150000 S TR DTC115EUA NPN (UMT3)) Location :PQ12 ADD (SCSB715F000 S SCH DIO RB715F UMD3) Location:PD20		
5	39	PWR-1.5VSP VCCPP	2009/08/04	COMPAL	Change the MOSFET to meet NECP rule	Change (SB00000DA00 S TR SI4634DY-T1-E3 1N SO8) to (SB00000LC00 S TR SI4166DY-T1-GE3 1N SO8) Location :PQ31 PQ35		
6	44	PWR-CPU_CORE	2009/08/04	COMPAL	Change the schematic to same with common circuitry	Change (SD028470280 S RES 1/16W 47K +-5% 0402) to (SD000009080 S RES 1/16W 1.91K +-1% 0402) Location :PR146		
7	46	PWR-VCC_GFXCOREP	2009/08/04	COMPAL	FOR INTESIL suggest to add 0 ohm resister	ADD (SD130000080 S RES 1/10W 0 +-5% 0603) Location :PR280 281		
8	48	PWR-0.75VSP/1.8VP	2009/08/04	COMPAL	ADD two posester for HW request	ADD(SL2000000S00 S THERM_ 470 +-50% PRF18BA471QB5RB 0603) Location :PR278 PR279		
9	46	PWR-VCC_GFXCOREP	2009/09/30	COMPAL	FOR HW POWER BUDGUT	Change (SB00000CG00 S TR A04466 1N SO8) to (SB0000008L80 S TR SI7686DP-T1-E3 1N POWERPAK SO8) Location :PQ43		
10	48	PWR-0.75VSP/1.8VP	2009/09/30	COMPAL	For HW power saving enable request	ADD(SB000009080 S TR SSM3K7002F 1N SC59-3) Location :PQ50		
11	46	PWR-VCC_GFXCOREP	2009/09/30	COMPAL	FOR HW POWER BUDGUT	Change (SB00000DA00 S TR SI4634DY-T1-E3 1N SO8) Location :PQ44	to (SB00000F000 S TR SI7170DP-T1-GE3 1N POWERPAK SO8)	
12	47	PWR-INV_9VP	2009/09/30	COMPAL	For customer adjust current limit	Change (SD021180D80 S RES 1W .018 +-1% 2512) to (SD021120D80 S RES 1W .012 +-1% 2512) Location :PR204		
13	48	PWR-0.75VSP/1.8VP	2009/09/30	COMPAL	For HW power saving enable request	ADD(SD034100280 S RES 1/16W 10K +-1% 0402) Location :PR282		
14	48	PWR-0.75VSP/1.8VP	2009/09/30	COMPAL	For HW power saving enable request	ADD(SD034100380 S RES 1/16W 100K +-1% 0402) Location :PR283		
15	39	PWR-Charger	2009/09/30	COMPAL	Change the CP point to 65W	Change (SD034100280 S RES 1/16W 10K +-1% 0402) to (SD034110280 S RES 1/16W 11K +-1% 0402) Location :PR62		
16	48	PWR-0.75VSP/1.8VP	2009/09/30	COMPAL	For HW power saving enable request	ADD(SE076104KN0 S CER CAP .1U 16V K X7R 0402) Location :PC228		

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Schematic	Rev.
1	48	PWR-0.75VSP/1.8VP	2009/09/30	NEC	For HW power saving enable request	ADD(SB0000009080 S TR SSM3K7002F 1N SC59-3) Location :PQ50		0.1
2	48	PWR-0.75VSP/1.8VP	2009/09/30	NEC	For HW power saving enable request	ADD(SD034100280 S RES 1/16W 10K +-1% 0402) Location :PR282		
3	48	PWR-0.75VSP/1.8VP	2009/09/30	NEC	For HW power saving enable request	ADD(SD034100380 S RES 1/16W 100K +-1% 0402) Location :PR283		
4	48	PWR-0.75VSP/1.8VP	2009/09/30	NEC	For HW power saving enable request	ADD(SE076104KN0 S CER CAP .1U 16V K X7R 0402) Location :PC228		
5	48	PWR-0.75VSP/1.8VP	2009/09/30	NEC	For HW power saving enable request	DEL(SE076104KN0 S CER CAP .1U 16V K X7R 0402) Location :PC200		
7	48	PWR-0.75VSP/1.8VP	2009/09/30	NEC	For HW power saving enable request	DEL(SD034100280 S RES 1/16W 10K +-1% 0402) Location :PR257		

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	20		7/28	NECP	NECP comment	Change Y13 from 8MHZ 20PF 50PPM X8A008000IK1H to 8MHZ 20PF +-20PPM X5H008000DK1H	0.2
2	31		7/28	Compal	Auto wake up	Connect EC_EMAIL_BTN to R1704 pull high	0.2
3	37		7/28	Compal	System can not wake on LAN	Del Q57 Add Q40, Q41, R772 on LV and VE model	0.2
4	28		7/28	Compal	System can not power on with BT	Change BT_DET# from PCH to ENE3810 GPIO06	0.2
5	10		7/28	Compal	DIMM II can not use	Change DIMMII_SAL from GND to pull high 10K ohm	0.2
6	21		7/28	NECP	NECP comment	Remove MSEN # and REF_GND	0.2
7	4		8/6	Compal	S3 Power Reduction	Add reset and Gate circuit for reduce S3 power consumption.	0.2
8	31		8/6	Compal	HQE button signal is NC	Connect to KB926 GPIO41	0.2
9	23		8/6	Compal	Power leakage from OZ888	Change U83 and U129 power source to +3VS and add Gate for MMI_LED	0.2
10	28		8/20	NECP-AI	TPM timing sequence	Add SUS_STAT# for meet TPM timing requirement and change TPM CONN	0.2
11	34		8/20	Compal	USB3.0 CONN	Add JUSB4/5 for co-lay USB 2.0/3.0	0.2
12	11, 21		8/20	NECP	SUPER I/O reference CLK	Add reference CLK for superIO from CLK_GEN	0.2
13	31		8/20	Compal	EC debug port	Add Tx/Rx from EC to Mini card2 for debug	0.2
14	37		8/21	NECP	NECP commet for MOS-FET Spec	Add the voltage divider and soft star circuit	0.2
15	31, 37		8/21	NECP-AI	iAMT timing requirement - M_PWROK<->VccLAN	Add SLP_M# signal control by EC and remove SLP_LAN to control +1.05VM power rail	0.2
16	34		8/21	Compal	USB EMI requirement	Add COMM-CHOKE for USB	0.2
17	23		8/24	NECP	OZ888 power sequence	Change Enable pin to +3VS	0.2
18	37		8/24	NECP	+5VM inrush current	Change C814 to 0.1uF	0.2
19	12		8/24	Compal	SATA port re-define for BIOS	Port 0:SSD; Port 1: HDD; Port 4:ODD; Port 5: eSATA	0.2
20	33, 34		8/24	Compal	USB 3.0 and e-SATA pin definition problem	Update JUSB1, JUSB2, JESATA CONN pin definition	0.2
21	34		8/24	Compal	UPD720200 boot-up sequence	Use USB_RST# to reset	0.2
22	22		8/24	Compal	Set up 4db for EQUALIZATION SETTING:	Change Pin 10,3,4 of ASM1442 to Low,High,High	0.2
23	15		8/25	Compal	Set up for distinguish SKU	Add pull down for GPIO 36 and GPIO 37	0.2
24	11,13,18, 23,26,34		8/27	NECP	NECP comment	Change X1,X1,Y4,Y5,Y11,Y12 to 20PPM	0.2
25	21		8/27	NECP	NECP comment	Add C7,C8 for EDID_CLK and EDID_DATA.	0.2
26	27		8/27	Compal	U87 will be EOL.	Co-lay U7 for tri-run.	0.2
27	23		8/30	NECP	NECP comment	Update OZ888 circuits	0.2
28	21		8/31	NECP	INV current protect	Change F3 to 5A	0.2
29	23		8/31	NECP	IO current protect	Add R115, R116, R117 posestor for NECP comment	0.2
30	36		9/01	NECP	Add for tune vgate falling-time	Add U131, R38 for NECP comment	0.2
31	23		9/01	NECP	Add for discharge	Add Q112, Q113 for NECP comment	0.2
32	34		9/01	NECP	USB	Add R118, R119, R120, R121 for USB2.0 layout	0.2
33	33		9/02	Compal	Wrong connection in USB port.	Switch signal of R1729,R1730	0.2
34	18		9/02	Compal	Add for EMI test	Add L7-L14	0.2
35	29		9/14	Compal	The power of WLAN card can't be turn on.	Add pull-high to WLANPW_DIS#	0.3
36	33		9/14	Compal	The signals of ESATA are swap.	Swap SATA_PTX_C_DRX_P4 and SATA_PTX_C_DRX_N4	
37	21		10/1	Compal	Already mount in sub board.	Remove form M/B	
38	18		11/2	Compal	Add L11-L18,delete R1945-R1965 (exclude R1952,R1957,R1963)		

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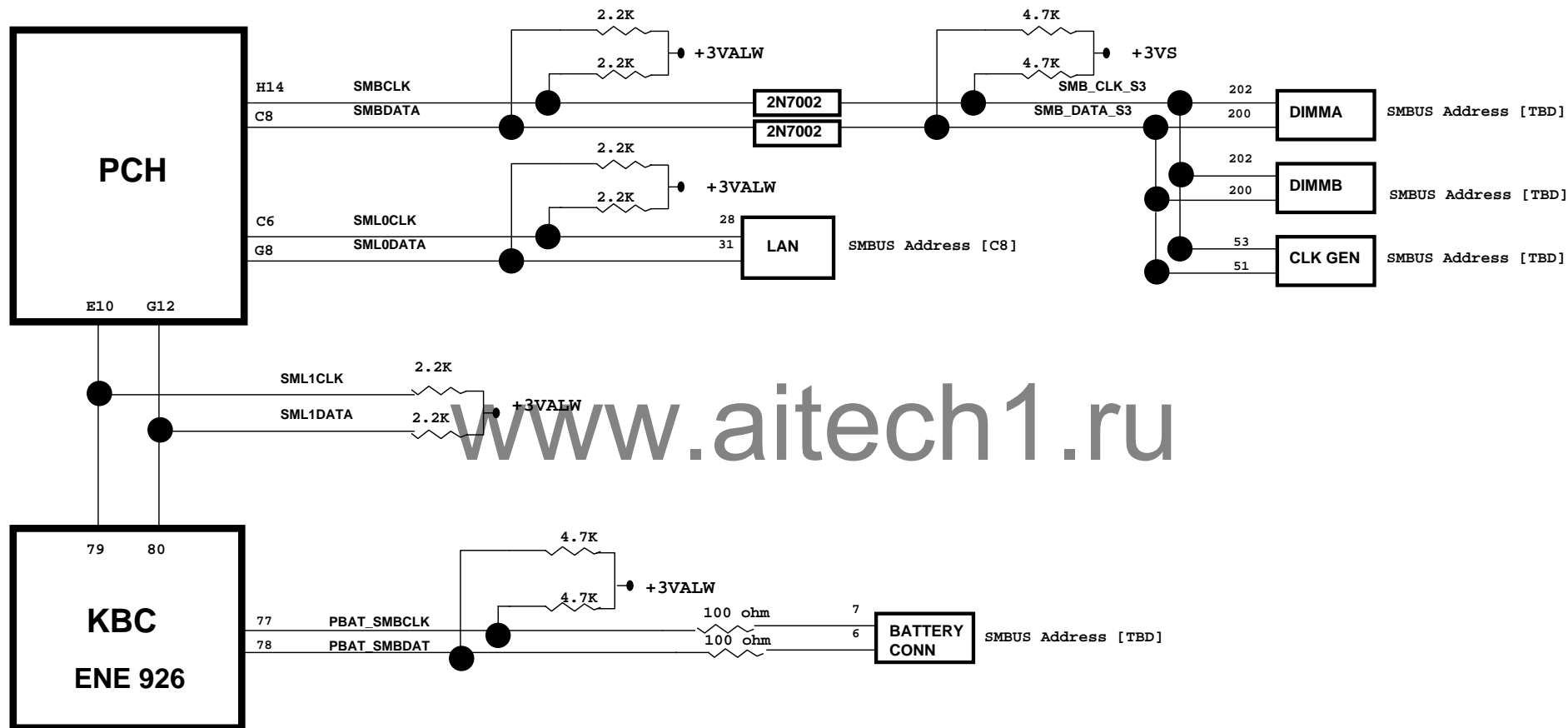
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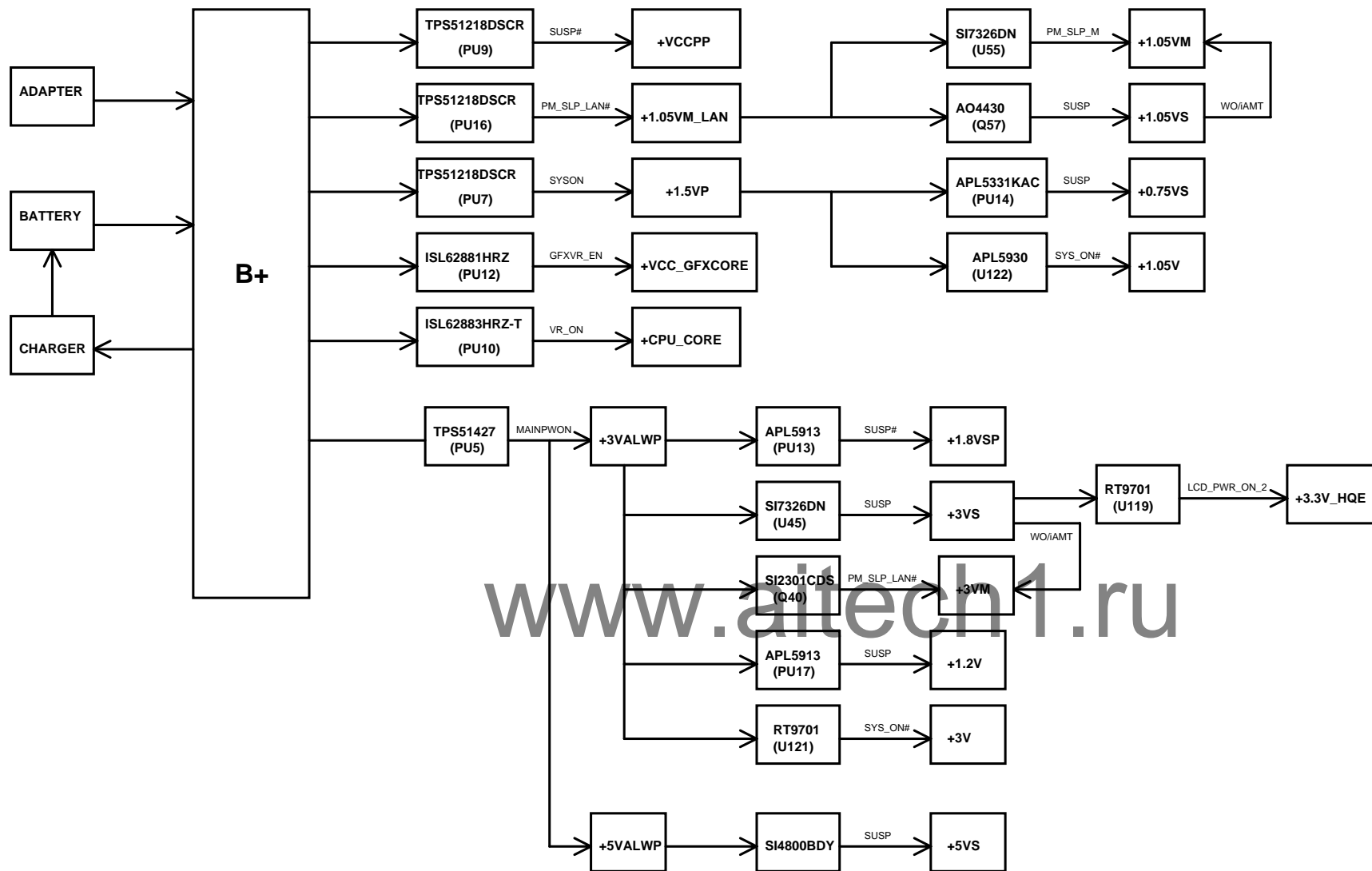
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1	22, 37, 45		10/26	NECP	System power on when insert AC	Change B+BIAS circuit	0.4
2	21		10/29	Compal	Remove reserve circuit	Remove reserve circuit: EMI reserve circuit	0.4
3	27		10/29	Compal	Remove Co-lay circuit	Remove Co-lay circuit: speaker trace	0.4
4	30		10/31	Compal	Remove Jump	Remove Jump: HDD/ODD power	0.4
5	34		10/31	Compal	USB3.0 power switch can not enable.	Change U104/U105	0.4
6	4, 5		11/3	Compal	Remove reserve circuit	Remove reserve circuit:XDP	1.0
7	21		11/4	NECP	Add panel ID for HQE	Add LCDCH_DET_2 signal to JLCD1 Pin19	1.0
8	30, 34		11/4	NECP	USB3.0 power switch	Add control signal USB3.0_EXTTPWR_OFF	1.0
9	35		11/4	NECP	Change WLAN LED power	Add resistor to JFUN1 Pin25	1.0
10	35		11/4	Compal	ESD protect	Add C15, C16 for ESD team recommend.	1.0
11	23		11/8	NECP	LED On immediately after Power turned On	Add U6, Delete R2012	1.0
12	13		11/8	Compal	BOM for USB3.0	Modify C1005,C1006,R2048 BOM for USB3.0	1.0
13	21		11/9	NECP	Display OFF circuit	Modify DISPLAY_OFF circuit to follow NECP recommend	1.0
14	30, 31, 34		11/9	NECP	Rename for Net	USB_EN# --> USB_EN; USB3.0_EXTTPWR_OFF --> USB3.0_EXTTPWR_ON	1.0
15	23		3/8	NECP	Some particular memory card can't be detected.	Change R2004 from 33 ohm to 0 ohm	1.0
16	30, 34		3/19	NECP	NEC comment	Use TEPSLD1A157M(40)12R for 150u capacitor.	1.0
17	33		4/8	NECP	Faildchild's bus-switch fail when EA test.	Use TS3USB221RSER for USB bus-switch	1.0
18	37		4/8	NECP	Abnormal auto-reboot happen when S3 test	Change RC timing to 36.5K and 2200P	1.0
19	21		4/8	NECP	2nd and 3rd source fail when EA test	Use 74ABCT1G125GW for H/V sync buffer	1.0
20	26		4/8	Compal	1.6mm of height is over 1.5mm of limit-height	Change C545 from 1.6mm to 1.25mm	1.0
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